Photolithographically Fabricated Sub-100 nm Silicon Slot Waveguide

Huijuan Zhang, Shiyi Chen, Junfeng Song, Haifeng Zhou, Chao Li, Ming Bin Yu, and Guo-Qiang Lo

***Abstract*—We propose a novel two-layer lithography method to fabricate sub-100nm slot using complementary-symmetry metal–oxide–semiconductor (CMOS) compatible processes. The slot waveguide is originally patterned using deep-UV photolithography (248nm) that has a resolution limit of 200 nm. A sacrificial etching technique is then employed to facilitate the nanoscale slot fabrication by film deposition and etching back. Sub-100 nm slot dimensions are successfully achieved in fabrication. The waveguides in the rest of devices are then patterned and obtained as per normal. By separating the lithography process into two-steps (one for slot and one for waveguide), we are able to fabricate 60nm slot with a high yield and throughput without interfering the device design. The presented technique is very useful for wide applications of slot waveguide, especially non-linear optics and modulator.**

***Index Terms*—Optical device, slot waveguide, CMOS-compatible fabrication, silicon photonics.**

I. Introduction

There has been intensive interest in slot waveguide [1] recently for its wide applications, such as light emitting device [8], modulator [9], sensors [11]], directional coupler [13] and polarization splitter [15]. In a slotted waveguide, a layer of low refractive index material is introduced between two layers of high refractive index material, to enhance the polarization sensitivity of the device. Basically, the slotted waveguides can be divided into two categories: vertically-oriented slotted waveguides for TE mode strong confinement and horizontally-oriented ones for the TM case. Horizontal slot waveguide has limited application due to its orientation. The paper here presents a novel fabrication technique for vertical slot waveguide specifically. The electric field discontinuity between the high index and low index region, will allow the TE polarized mode to remain highly confined to the low index region by principle of total internal reflection. The dimension (width) of a slot on Si-on-insulator (SOI) platform is preferred to be sub-100 nm so that to better confine light in the low index region enabling the aforementioned applications, which is not achievable for deep ultraviolet optical lithography system. Electron beam lithography followed by dry etching [1],[16] or Focused Ion Beam etching [17] is often used to obtain sub-100 nm slot dimension. These techniques are in a series manner and hence very slow and ineffective. A CMOS compatible-process is then much desired for Si-based slot waveguide fabrication that will allow high volume manufacturing. Here we present a CMOS-compatible approach to achieve sub-100 nm slot waveguide by conventional 248 nm optical lithography.

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II. Device Design

The slot structure was firstly proposed by Almeida *et al.*[1] The optical mode in such a structure tends to propagate mainly within the center of the slot. The essential feature of a Si based slot waveguide is two silicon stripes formed by etching an SOI slab and separated by nanoscale spacing, *i.e.* a slot as shown in Fig. 1a). Optical simulation was carried out by using three-dimensional finite-difference-time-domain (3D-FDTD) in Rsoft. The operating wavelength is 1550 nm. The waveguide core is Si with an index of 3.5, while the cladding is silicon dioxide (SiO_2) with an index of 1.45. The Si thickness is 340 nm and waveguide width is 500nm.

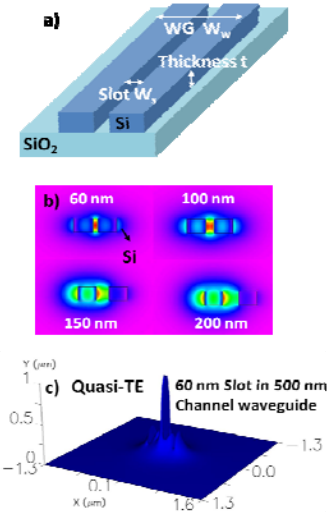

Fig. 1. a) Schematic drawing of a slot waveguide. width of the slot and waveguide in total is denoted as W_s and W_w. The thickness of the Si is t. b) Fundamental TE mode profiles in slot waveguide when t =340 nm. W_W= 500 and W_s = 60, 100, 150 and 200nm, respectively. c) Mode confinement of TE in slot waveguide when W_W= 500 and W_s = 60nm.

Fig.1b) is the optical field distributions for quasi-TE mode when slot width is 60, 100, 150 and 200nm, respectively. The major E-field component is perpendicular to the Si/slot interface. Large discontinuity and high E-field confinement in the low-index SiO_2 slot region is observed as shown in Fig. 1c). The effective refractive index (n_{eff}) when slot is 60nm is equal to 1.96. It is observed that the mode is no longer

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confined in the slot region due to the high index contrast if slot is too wide (above 100nm).

Due to the higher propagation loss of the slot waveguide than the conventional channel waveguide, we minimize the total length of the slot waveguide in our circuit design by only using slot waveguide in the functional part while using conventional channel waveguide for light propagation elsewhere. Therefore, there will be two junctions for mode coupling from channel waveguide to slot waveguide (in) and slot waveguide to channel waveguide (out). To study the insertion loss due to mode mismatch between the slot mode and the channel mode, we simulate the mode transition using 3D-FDTD. (Fig. 2) The optical simulation shows a total loss of 0.77 dB for a pair of junctions (in and out) with parameters of W_s= 60 nm and W_W = 500 nm.

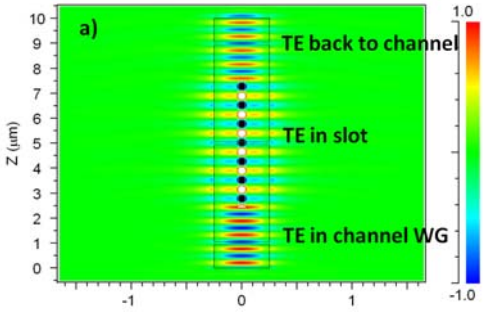

Fig. 2. Light propagation from a channel waveguide into a slot waveguide and then back to channel waveguide. Power monitors were placed at the input waveguide and the output end to study the insertion loss.

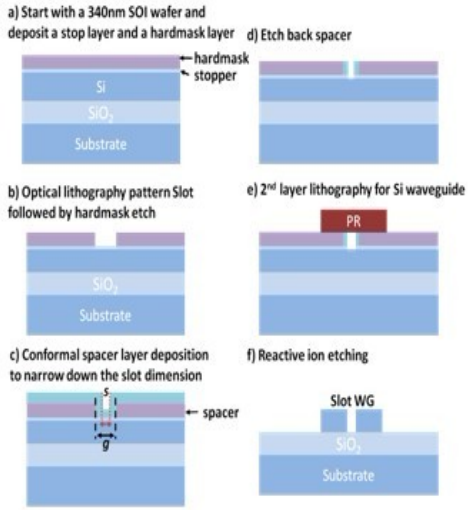

Fig. 3. Fabrication process flow.

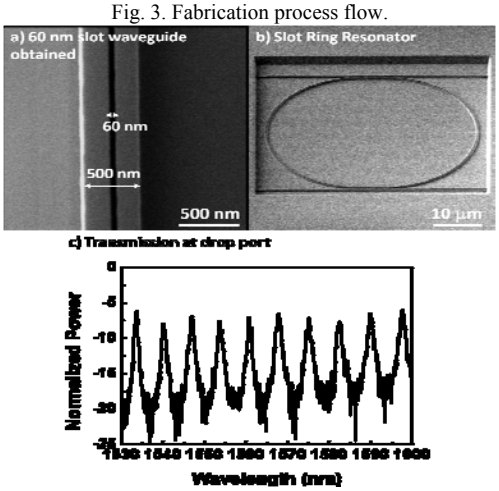

Fig. 4. SEM images of a) 60 nm slot waveguide and b) slot ring resonator in a SiO_2 window. c) Transmission spectrum at drop port.

III. Fabrication

It is noted that the resolution limit of deep ultraviolet optical lithography system (248 nm) is about 200 nm, which is not sufficient to fabricate the desired slot dimension. A CMOS-compatible method is reported here to overcome this lithographic resolution limit and achieve sub-100nm slot waveguide by making use of sacrificial layer deposition and etching without using EBL or FIB. The fabrication process flow is illustrated in Fig.2. The method starts with a SOI wafer with active Si layer having thickness of 340 nm. A 300 A silicon oxide (SiO_2, functions as a stopping layer) layer is deposited to a cleaned substrate followed by 1200 A silicon nitride (Si_3N_4, hardmask) layer deposition in plasma-enhanced chemical vapor deposition system (PECVD). (Fig. 3a) After optical lithography, slot pattern with a width g is patterned and transferred to the hardmask by Si_3N_4 etch and stops at the SiO_2 surface so that the beneath Si layer remains untouched. (Fig. 3b) A conformal layer, here we use Si_3N_4 for this sacrificial layer (named as spacer), is then deposited on the patterned wafer to narrow down the patterned gap g from lithography to dimension s. (Fig. 3c) The spacer layer is then etched back to leave a narrowed slot. (Fig. 3d) Next, the waveguide pattern is defined by second layer of lithography. (Fig. 3e) Finally, the waveguide and slot Result and Discussion

Fig. 4a) shows a scanning electron microscope (SEM) image for a Si slot waveguide obtained after Si etching and hardmask stripping. The slot has a dimension of 60 nm and the width of waveguide remains 500nm. The device dimension is very uniform across an 8" wafer. This slot width is not achievable using conventional 249nm or even 193nm optical lithography. In the proposed technique, the slot fabrication is decoupled from the waveguide fabrication by using a two-layer optical lithography for slot and waveguide separately. In this way, the waveguide dimension is not affected during the spacer deposition and etched back. It is an improvement from our previous work. [18]

To characterize the slot waveguide loss, several waveguides were fabricated with various lengths, ranging from 50 to 1000 μm in length. The result shows a waveguide propagation loss of 16.7 dB/cm, which is slightly worse than our previously reported value 11.1 dB/cm in Ref[12], possibly due to the narrower slot than previous 100 nm slot. The major portion of loss should come from edge roughness and material absorption as slot waveguide is relatively more sensitive to the edge roughness than normal channel waveguide due to the high light intensity in the slot region. Further improvements on reducing the waveguide propagation loss may be achieved by thermal oxidation follow by oxide stripping using wet etch, which is known to be able to smoothing sidewalls. [19] The channel-slot coupler loss is measured to be about 1.18 dB/pair, which is also higher than the simulation result. The discrepancy should be resulted from the reflection at the slot-channel junction and impact sidewall condition in the real device.

To demonstrate the integration capabilities of the slot waveguides, a ring resonator structure was fabricated with the slot waveguide. SEM image of a ring resonator having a 30μm diameter in oxide window is shown in Fig. 4b). Its

transmission spectrum at the drop port is shown in Fig. 4c). The Q-factor is calculated to be about 1628. This performance should be improved if the waveguide propagation loss is further reduced.

IV. Conclusion

In conclusion, we report a CMOS-compatible approach to fabricate sub-100 nm Si-based slot waveguide in wafer-scale production. The approach allows wafer-scale mass production for slot waveguide. The proposed method includes a key step of sacrificial spacer layer deposition before conventional waveguide etching so that the pre-patterned slot dimension is narrowed down to obtain sub-100nm slot. Finally, a ring resonator structure is demonstrated. The high optical field concentration in the slot region will be very advantageous when compared to conventional Si waveguide, in particular, for nonlinear optics and modulation applications.

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