Design and Analysis of Low Power and High Speed Dynamic Latch Comparator in 0.18 μm CMOS Process

Raja Mohd. Noor Hafizi Raja Daud, Mamun Bin Ibne Reaz, and Labonnah Farzana Rahman

***Abstract*—A novel design of CMOS dynamic latch comparator with dual input single output with the differential amplifier stage is presented. The designed dynamic latch comparator is required for high-speed analog-to-digital converters to get faster signal conversion and to reduce the power dissipation, which is immune to noise than the previous works. In this paper, the design and analysis of a latch comparator using charge sharing circuit topology is illustrated to achieve low power and high-speed operation. The proposed circuit is designed using 0.18μm CMOS process. The simulated results shows that 100 MHz clock frequency with the power supply voltage (VDD) 3.3V and input range 3.3V produce the desired output signal. The topology of the proposed design is able to minimize the propagation delay and power consumption with the improved performances than other research works. Moreover, the different capacitor value and the transistor lengths produced the faster output, which is suitable for the successful operation of the ADC.**

***Index Terms*—ADC, dynamic latch comparator, charge sharing, CMOS, low power, high speed.**

I. Introduction

A comparator becomes the great electronic device, which widely used in the analog to digital converters and plays important role in high speed ADC. An important circuit that is used for transition the analog to digital signal is the comparator. In general, a comparator is a device, which compares two currents or voltages and produces the digital output based on the comparison. Many applications, such as analog to digital converters (ADCs), memory sensing circuits and recently also on chip transceivers are widely using comparators [1]. In the last years, most of the researches focus on the comparator with low power consumption, simple thermal management and high efficiency. The growth of the portable electronic devices makes the power consumption is critical issue to circuit designers because the low power and high speed comparators are the main building block in the front end of the radio frequency receiver in the most of the modern telecommunications system [2].

Recently, most of the researchers have proposed the dynamic latch comparators based on the cross coupled inverters to provide the latching in order to force a fast decision due to the positive feedback commonly used in flash analog digital converters (ADCs) due to their high decision speed. Fig. 1 shows a widely used standard conventional latch type comparator circuit with the high impedance input, rail to rail output swing and no static power consumption [1]. Robustness against noise and mismatch are the main advantages of the conventional latch type comparator. However, it suffers from high sufficient power supply, which is caused by many stacked transistors in circuit design.

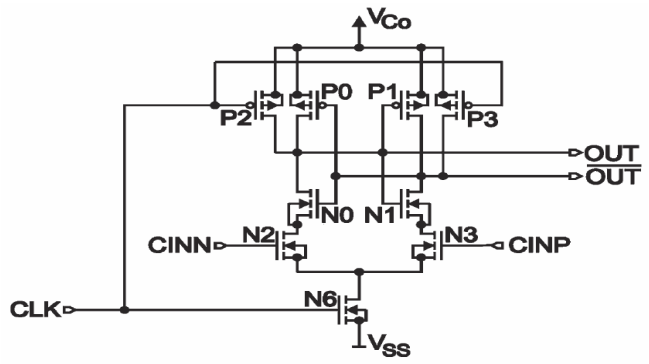

Fig. 1. Conventional latch-type comparator.

Goll and Zimmermann proposed a comparator with reduced delay time in 65nm CMOS using 0.65 V as the supply voltages as shown in Fig. 2 [1]. The proposed design is different from the conventional circuit by replacing a new latch for low power supply voltage operation, which offers the great advantages of high impedance input, a rail to rail output swing, no static power dissipation and indirect influence of the parasitic capacitances of the input transistors to the output nodes.

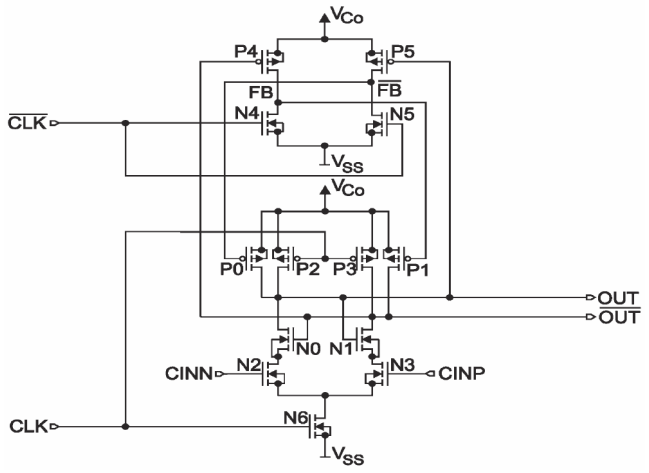

Fig. 2. Comparator with modified latch.

In this paper, a new CMOS dynamic latch comparator is presented. The fully dynamic charge sharing topology employed latch circuit with high input impedance. Moreover,

Manuscript received August 3, 2012; revised September 3, 2012.

Raja Mohd. Noor Hafizi Raja Daud is with the Universiti Kebangsaan Malaysia, 43600 Bangi, Selangor, Malaysia.

The authors are with the Universiti Kebangsaan Malaysia, 43600 Bangi, Selangor, Malaysia. (e-mail: mamun.reaz@gmail.com).

a rail to rail output swing is produced with no static power dissipation. In addition, the proposed designed comparator is free from indirect influence of the parasitic capacitances of the input transistors to the output nodes. The design is optimized by choosing the right W/L ratio of the transistors in the circuit. The new design exhibits latched MOS transistors with faster output.

II. Methodology

The technology of scaling of MOS transistors improves the high speed and low power operation, the offset of the comparator in increased owing to transistor mismatch. Jung et al. proposed the low power and low offset comparator using latch load as shown in Fig. 3, which using the dynamic offset cancellation and latch load is to reduce the power consumption and offset voltage of the comparator [3]-[5].

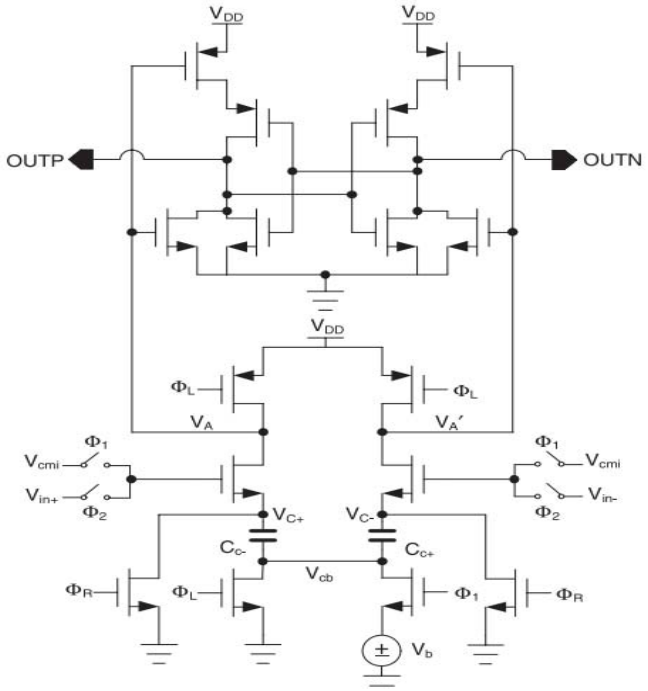

Fig. 3. Low power and low offset comparator using latch load.

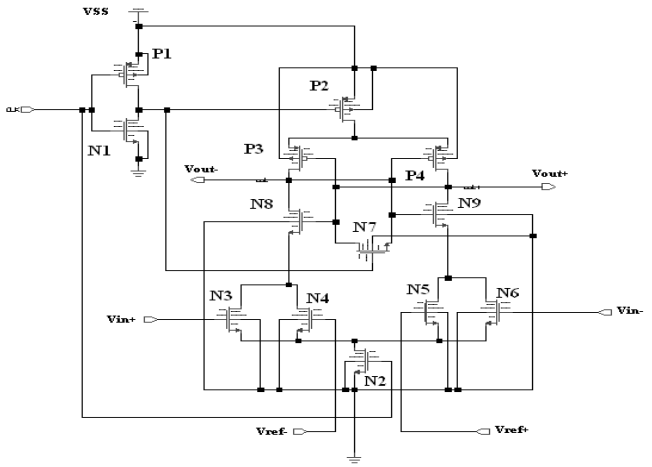

Fig. 4. Proposed design of comparator circuit.

The topology of the proposed comparator circuit as shown in Fig. 4 describes about the charge sharing comparator combines the positive features of the previously designed dynamic latch comparator, which can be used in pipeline A/D converter. The proposed designed dynamic latch comparator is the combination of resistive dividing comparator and differential current sensing comparator.

The complete layout of proposed designed comparator circuit is shown in Fig. 5 using the CEDEC 0.18 um CMOS process. The layout area of the circuit is minimized by sharing the drain and source connection between the MOSFETs. The capacitors are not located in layout because to reduce the cost of the whole chip. Moreover, the capacitor is put in the test bench of the circuit.

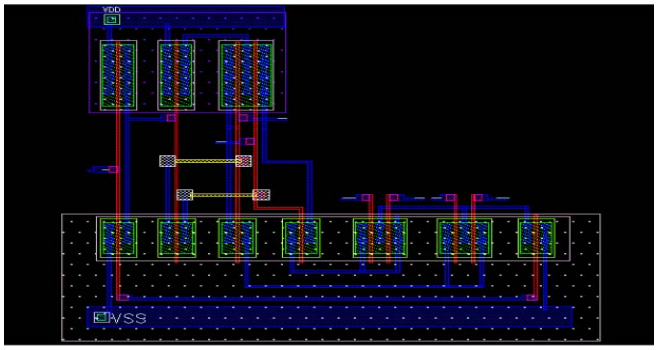

Fig. 5. Layout of the proposed design.

III. Simulation Results and Discussion

CEDEC 0.18-µm CMOS process is used to measure the output results of the proposed dynamic latch comparator circuit with the ELDONET simulator. The input voltage Vin is set to 3.3 V and the reference voltage Vref is set to 1.65 V for simulating the outputs. 27oC operating condition is used for the proposed dynamic latch comparator circuit. The critical design parameters for designing the proposed CP circuit are listed in Table I.

TABLE I: Main Design Parameters

Parameters	Value
Voltage input (Vin)	3.3 V
Voltage reference (Vref)	1.65
All MOS Transistor length	0.18 µm
PMOS width	6 µm
NMOS width	3 µm

The basic comparison between the comparator waveforms should be functional. If the input of the comparator is greater than the reference voltage, Vref, then the output results will be a "1" and if the input voltage is less than reference voltage then the output voltage of the comparators produces output of "0." The waveform as shown at Figure 6 is the required function, which is efficiently be produced by the comparator. The most important dynamic parameters that determine the speed of a comparator are the propagation delay and the settling time [6].

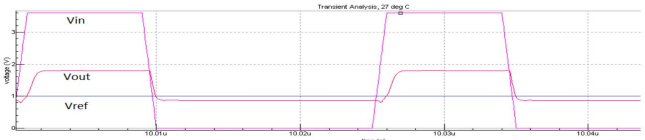

Fig. 6. Comparator waveform in vin,vout and vref.

The simulated waveform, which is produced by the

proposed dynamic latch comparator, is shown in Fig. 7 and the width and the length of the transistor used in the design process of the comparator circuit is shown in Table II.

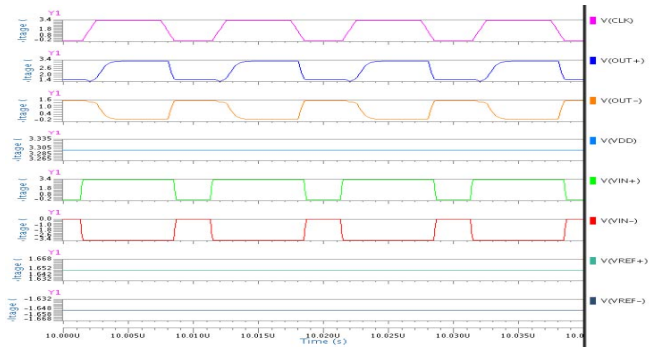

Fig. 7. Simulation results of proposed design comparator.

TABLE II. TRANSISTORS PARAMETERS FOR PMOS AND NMOS

Transistors	Length	Width
PMOS	0.18 µm	6 µm
NMOS	0.18 µm	3 µm

The operation process of the dynamic latch comparator to produce the output waveform is shown in Fig. 8. The output voltage is changing from logic '0' to logic '1' when the input voltage Vin+ larger than reference voltage *Vref*+.

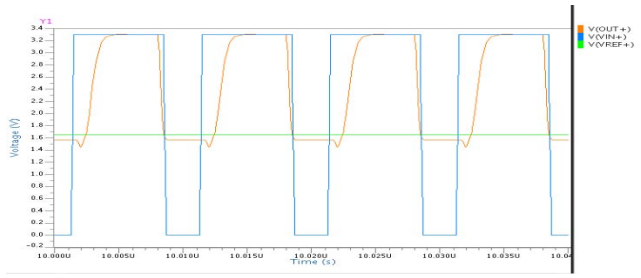

Fig. 8. The waveform of vout+ based on vin+ and vref+

On the other hand, when *Vref*+=*Vref*-=1.65V and *Vin*+=*Vin*-=3.3V are twice the *Vref* produced the waveform of the *Vout*+ along with the *Vout*- in square waveform is shown in Fig. 9.

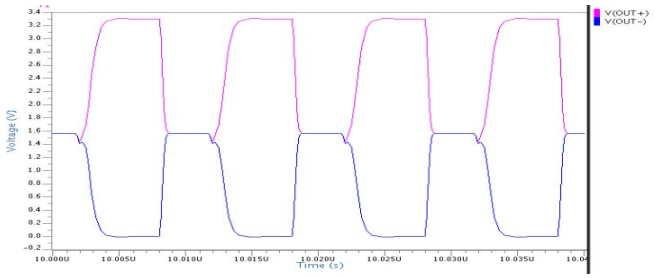

Fig. 9. The waveform of dynamic latch comparator

The load capacitor significantly reduces the noise at the output voltage because it acts to remove the ripple from the power supplies and to store energy or electrical charge. Moreover, capacitor is used to resist any change of voltage across due to capability to store a charge and gives the output voltages waveform smoother. Fig.10 shows the faster output waveform with small value of the capacitor, which is produced when the value of the capacitor is decreased [7]. Hence, the proposed designed dynamic latch comparator uses 0.5pF capacitor as load.

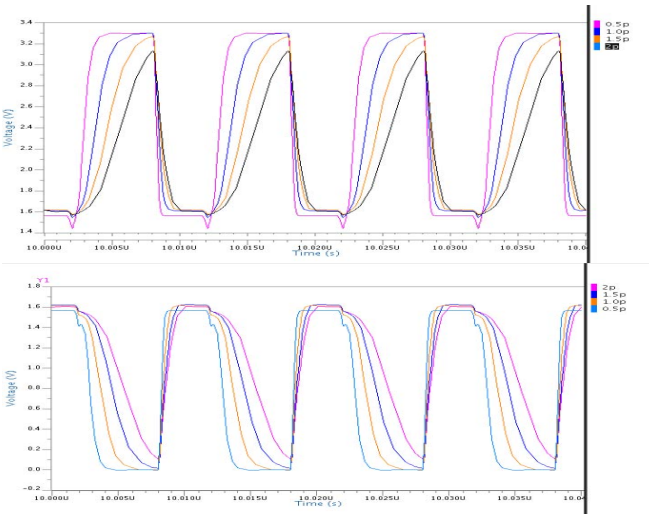

Fig. 10. Output waveform with different capacitor value.

The length of the MOS transistors also influences the capability of the comparator to generate the faster output. The waveform output with different length of transistors is shown in Fig. 11. The smaller length 0.18 um will produces the faster output with higher speed due to less propagation delay compared to the 0.20 um, 0.22 um and 0.24 um. All the PMOS and NMOS transistors used in the proposed designed is 0.18um.

Although the smaller width of transistors will reduce comparator operation speed but the area can be reduced to more compact and low cost.

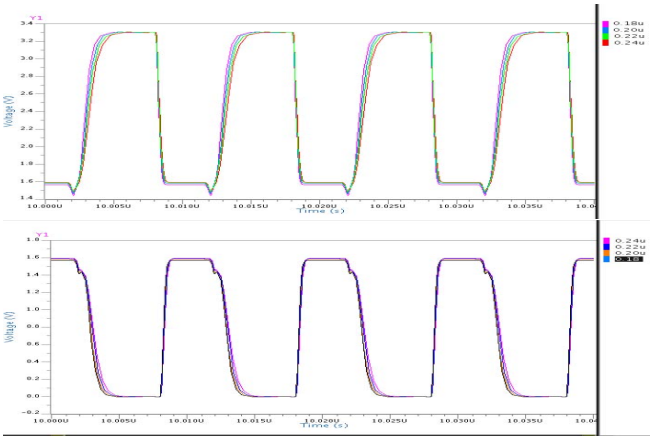

Fig. 11. Simulated output waveform with different length transistors

IV. CONCLUSION

In this paper, a new dynamic charge sharing topology is used to optimize the parameters for high speed applications. Designing dynamic latch comparator has its own pros and cons where optimization of one or more parameters may easily result in degradation of others. The main challenge lies on the constant speed, which makes more critical. In this paper the faster speed has been gained by the proposed designed dynamic latch comparator with the combination of resistive dividing comparator and differential current sensing comparator. The simulated output showed that the proposed designed dynamic latch comparator is able to produce higher

speed with the power supply voltage 3.3 V. The proper scaling of MOS transistors provides the high speed and low power dissipation. Moreover, the smaller value of the capacitors and length of MOS transistors makes the novel designed dynamic latch comparator compatible for higher speed ADC applications.

REFERENCES

[1] B. Goll and H. Zimmmermann, "A Comparator with Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65V," *IEEE Transactions on Circuits and System II: Express Brief*, vol. 56, no. 11, pp. 810-814, Nov 2009.

[2] Y. Guo, W. Cai, and T. Lu, "A Novel 1GSPS Low offset Comparator for high speed ADC," *in Proc. Fifth International Joint Conference on INC,IMS and IDC*, Seoul, Korea, Aug. 25 -27, 2009, pp. 1251–1254.

[3] Y. Jung, S. Lee, J. Chae, and G. C. Temes, "Low-power and low-offset comparator using latch load," *Electronics Letters*, vol. 47, no. 3, pp. 167-168, Feb. 2011.

[4] M. Miyahara and A. Matsuzawa, "A low-offset latched comparator using zero-static power dynamic offset cancellation technique," in *Proc. IEEE Asian Solid State Circuit Conference*, Taipei, Taiwan, Nov.16-18, 2009, pp. 233–236.

[5] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid State Circuit Conference (A-SSCC)*, Fukuoka, Japan, Nov.3-5, 2008, pp. 269–272.

[6] R. S. Gamad and S. Kale, "Design of a CMOS Comparator for Low Power and High Speed," *International Journal of Electronic Engineering Research*, vol. 2, no.1, pp. 29-34, 2010.

[7] R. S. Gamad, P. Meena, "Low Power and High Speed CMOS Comparator Design Using 0.18μm Technology", *International Journal of Electronic Engineering Research*, vol. 2, no. 1, pp. 71-77, 2010.