

Wavelength-Agile Silicon Photonic Integrated Circuit for Low-Cost Optical Receiver

Chao Li, Huijuan Zhang, Shiyi Chen, Jing Zhang, Ning Duan, Mingbin Yu, and G. Q. Lo

Abstract—We report our recent work on wavelength-agile silicon photonic integrated circuit for low-cost optical receiver, which includes a monolithic integrated germanium p-i-n photodetector and a tunable filter. The circuit is fabricated using standard CMOS technology on SOI platform, paving the way for further integration with more optical building blocks and CMOS transistor circuits. The wavelength tuning range of the integrated circuit is ~11.5 nm along with the tuning speed of less than 400 μ s. The tuning efficiency is ~0.16 nm/mW. The measured fiber-to-PD responsivity of the photonic integrated circuit is ~0.10 A/W. A photonics packaging structure for the silicon PIC is also proposed.

Index Terms—Silicon photonics, integrated optics, optical waveguide, Germanium.

I. INTRODUCTION

In recent years, silicon photonics has seen substantial technological achievements beyond early expectations. Low loss high-index contrast silicon nanowire waveguides that can be fabricated by standard CMOS-compatible processes are showing promise for realistic dense photonic integrated circuit (PIC) [1]-[3] in various applications including optical communications, optical interconnects, signal processing and sensing. Compared with hybrid integration, the silicon PICs can significantly reduce the device footprint and packaging cost of optical communications modules.

Silicon has been known to be inappropriate as the material for the photodetector (PD) at telecommunication wavelength. However, recent research progress already demonstrated that germanium (Ge), which is compatible with current CMOS fabrication technology, becomes an attractive material for high performance near-infrared photodetector due to its favorable absorption coefficient [4]–[6].

Recently, the demand for high bandwidth connectivity to the home has been continuously growing with the increasing popularity of HDTV, 3D displays, and peer-to-peer file sharing. Global Fiber-to-the-Home (FTTH) deployments occur at a rapid pace and Asia Pacific market leadership expected to continue in the next few years [7]. Developing the wavelength agility for the optical communications network components can help reduce traffic congestion and optimize network bandwidth utilization by switching channels.

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Here we report our recent work on wavelength-agile monolithic integrated silicon PIC for optical receiver based on a polarization independent optical tunable filter and a Ge p-i-n PD using CMOS-compatible fabrication process.

II. DEVICE DESIGN

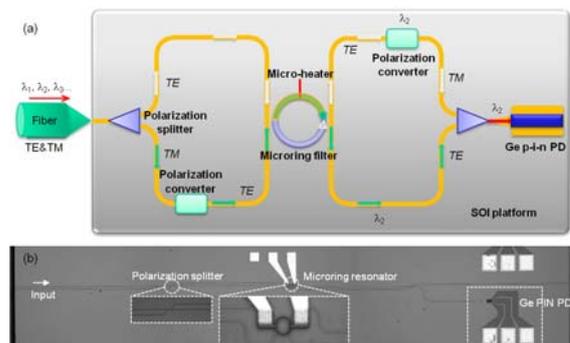


Fig. 1. (a) Schematic of the wavelength agile silicon PIC. (b) Top-view optical micrograph of the fabricated chip. Inset shows the zoom-in view image of the fabricated microring resonator.

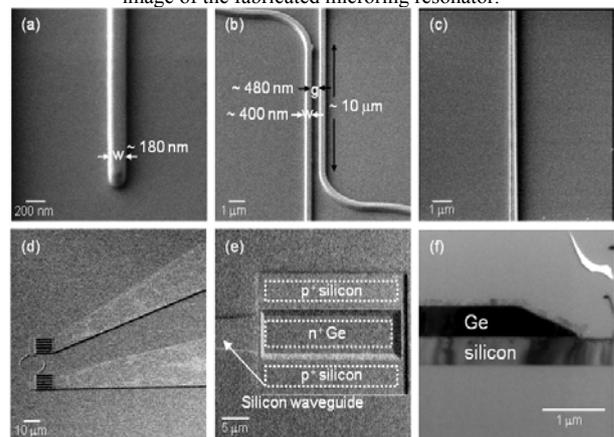


Fig. 2. (a)–(e) Scanning electron micrograph (SEM) of the invert tapered mode size converter, the mode-coupling based polarization splitter, the main transition region of polarization rotator, the TiN micro-heater with Al electrodes and the Ge PD. (f) Cross-section transmission electron micrograph (TEM) of the Ge PD.

Fig. 1 (a) illustrates the schematic of the wavelength-agile silicon photonic integrated circuit based on microring resonator and Ge p-i-n PD. By employing the polarization diversity scheme, we realized the polarization independent property for the silicon PIC, which is strongly desired in optical transmission system. The whole circuit comprises of two function building blocks. One is the polarization independent optical tunable filter to realize the wavelength agility; the other is the integrated Ge p-i-n PD. The design of the silicon polarization independent tunable filter is explained in [8]. Two sets of polarization splitters and polarization converters were employed in the circuit (shown

in Fig. 1(a)). The TE/TM polarization components of the input lightwave will be separated into two waveguide paths by the polarization splitter. Then one polarization state will be rotated to the other by the polarization converter so that only single polarization (TE) from both paths is achieved at the microring resonator filter where the signal at resonance will be dropped to the right-hand paths. Similarly, the rotated TM signal through the other polarization converter is then combined with the TE signal from the other path. At last, the light is evanescently coupled to the Ge vertical p-i-n PD through the silicon waveguide. Since the whole circuit is monolithically integrated on the SOI platform, it is possible to eventually include the electric IC on the same chip to achieve low-cost compact device. Figure 1(b) shows the top-view optical micrograph of the fabricated device. The insets show the zoom-in view of the microring resonator with the micro-heater on top and the Ge p-i-n PD.

III. DEVICE FABRICATION

The entire silicon PIC was fabricated on an 8-inch 400-nm-thick SOI wafer with 2- μm -thick buried oxide layer using CMOS-compatible technology. The device layout was defined by 248-nm Deep UV photolithography and transferred onto the device layer by dry etching. A 500-nm-thick epitaxial Ge layer was selectively grown as the active layer of the p-i-n PD [10]. Phosphorous and boron dopants were implanted to form the n+ region in Ge and p+ region in silicon. In order to form the ohmic contacts, the dopants were activated using rapid thermal anneal at 750°C for 3 minutes. A 600-nm-thick oxide layer was then deposited as an electrical isolation layer for the PD. After opening the contact holes on the PD, an 800-nm-thick metal layer was deposited and patterned as the first electrical connection layer. Then a 3.2- μm -thick oxide layer was deposited and polished by chemical mechanical polishing (CMP) to flatten the surface of the wafer, which is desirable for the following fabrication process. The micro-heater for wavelength tuning was made from high resistivity material TiN of 120 nm thickness and 1 μm width. After the micro-heater patterning and etching, another 500-nm-thick oxide cladding layer was deposited. The contact holes for the micro-heater and the PD (to connect the first metal layer) were then opened, followed by the 1- μm -thick metal layer deposition and patterning to form the electrodes.

Fig. 2(a) – (e) show the scanning electron micrograph (SEM) of the invert tapered waveguide mode size converter, the mode-coupling based polarization splitter, the main transition region of polarization rotator, the TiN micro-heater with aluminum electrodes and the Ge PD. Figure 2(f) shows the cross-section transmission electron micrograph (TEM) of the PD.

IV. DEVICE CHARACTERIZATION

After the fabrication, the opto-electrical response of the integrated device was characterized by using a tunable laser (Agilent 8164B) and a semiconductor analyzer (Agilent B1500A). The input optical power is ~ 0 dBm (1 mW). We

then measured the photocurrent of the integrated Ge PD by applying reverse bias voltage of 5 V while tuning the wavelength of the laser output by applying voltage on the optical tunable filter. We observed almost uniform peak transmittances (photocurrent of the integrated PD as shown in Fig. 3(a)) with various voltages upon the optical tunable filter. The measured free spectral range (FSR) of the microring resonator filter is ~ 11.5 nm. Upon 3.8 V applied voltage, the resonance “*” of the filter (1536.86 nm at zero voltage) was tuned 10.13 nm towards the longer wavelength (red-shift). The tuning range of the silicon optical tunable filter is able to cover the whole FSR with the tuning efficiency of ~ 0.16 nm/mV. We obtained the fiber-accessed responsivity of ~ 0.10 A/W (from the fiber to Ge PD through the optical tunable filter) at a reverse bias voltage of 5 V, which is corresponding to the fiber-to-PD loss of ~ 9.6 dB. The total loss includes the fiber-to-waveguide coupling loss of ~ 2.5 -3 dB, polarization splitter induced loss of ~ 2 dB, polarization converter insertion loss of ~ 2 dB, and waveguide propagation loss of ~ 1 dB. The polarization dependent loss of ~ 0.5 dB for the output electrical signal from PD between TE and TM polarization states at the peak wavelengths was observed. The 3-dB bandwidth of the PD response was characterized to be ~ 20 GHz at a reverse bias voltage of 5 V by an Agilent PNA Network Analyzer (E8363C).

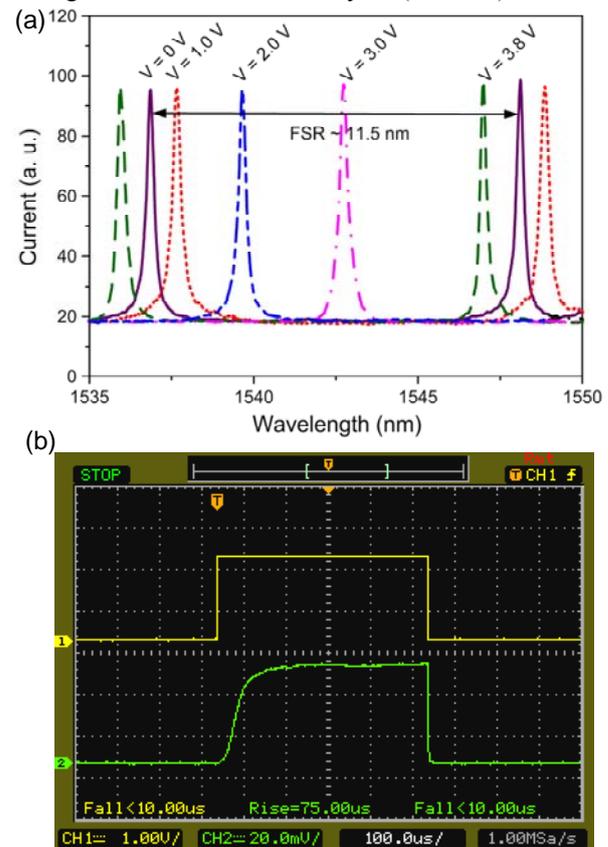


Fig. 3. (a) Opto-electrical spectrum response measured at Ge p-i-n PD for TE polarization with various voltage upon the silicon optical tunable filter. (b) 2 MHz electrical waveform and the resulting optical waveform of the silicon optical tunable filter.

We also characterized the wavelength tuning speed of the circuit by applying a 2 MHz square-wave electrical driving signal on the micro-heater. Figure 3(b) shows the driving electrical waveform with 0 – 3 V signal levels and the resulting optical waveform at 2 MHz modulation. The rise

time is $\sim 75 \mu\text{s}$ and the fall time is $\sim 1 \mu\text{s}$. The longer rise time suggests that the heat up process is slower than the heat dissipation. However, for practical usage, it will take longer time for the device to reach the thermo equilibrium state in order to achieve stable output at the desired wavelength. From the measurement, we could estimate the tuning speed of less than $400 \mu\text{s}$ in a conservative way.

We then proposed to employ the well known laser welding technique for the photonic packaging of the chip with fiber assembly. Among different techniques for silicon photonics packaging, laser welding packaging has the potential to be a promising method as it offers better strength, cleanliness, and long-term reliability. Fig. 4 depicts the proposed architecture of the device packaging. In order to achieve efficient coupling to the silicon chip, lensed fiber will be employed.

V. CONCLUSION

A wavelength-agile silicon photonic integrated circuit for optical receiver was reported. The monolithic integrated PIC was fabricated using standard CMOS technology on SOI platform. The silicon PIC demonstrates wavelength-agile capability. A fiber-accessed responsivity of 0.10 A/W was obtained at the reverse bias voltage of 5 V for the PIC. A packaging structure for the silicon PIC was also proposed.

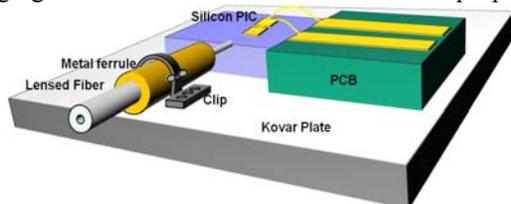


Fig. 4. Proposed schematic of the packaging structure.

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