II. DEVICE UNDER TEST

HfO$_x$ based RRAM devices used for this study are fabricated using the standard CMOS platform technologies on 8 inch Si wafers. 20 nm thick Ti and 50 nm thick Pt are firstly deposited by the E-beam evaporation as the adhesion layer and the bottom electrode, respectively. Then 10 nm HfO$_x$ and 50 nm TiN were deposited by reactive sputtering with proper annealing conditions as the respective switching layer and top electrode. Devices were then patterned with lithography and dry etched into the square shape with dimensions from 10×10 µm$^2$ to 100×100 µm$^2$. Post metal dielectrics were used to cover the wafer preventing devices from further possible damages after fabrication.

To compare DC current levels in the devices with different areas, small bias voltage sweep is applied in the states of fresh, HRS and LRS respectively. Voltage below transition threshold is used to avoid resistive switching during measurement. To get a clearer picture of the resistance levels at different states with device area scaling, Fig. 2 is plotted. It is seen that in the graph, HRS resistance is very similar to that of fresh device, which indicates a roughly complete recovery of conduction filament during reset process. More than that,
it shows a linear scaling resistance with device area in fresh and HRS states with log-log scale, while resistance keeps nearly constant at all device area points, which is believed to be related to compliance current level during set operations.

Fig. 2. Resistance versus device area plot for fresh, HRS and LRS. For both fresh and HRS state, resistance shows a reciprocal scaling effect with respect of device areas; while for LRS, there is no dependence on device areas.

Noise measurement are carried out on three states of device, fresh, HRS and LRS, and normalized power spectral density (PSD) with current is plotted in Fig. 3 under different bias conditions. It is seen that for all three states, PSD slopes are close to 1, which confirms the 1/f noise nature for the oxide-based RRAM devices. It can also be seen from the figure that the noise PSD is independent of bias conditions, which means it is an intrinsic characteristic of the current conduction.

Fig. 4 is the PSD spectrum of HRS state from L10 to L100. It is seen that the noise PSD scales reciprocally with the area (similar to the observation in CMOS devices). To compare L10 with L100, a PSD level difference of around two orders of magnitude is observed. However, after normalizing with the device area, the four PSD curves fall into a similar level, as illustrated in Fig.

Unlike fresh or HRS, LRS current conduction is localized with conduction filament; as so, LFN spectrum is expected to be independent of device areas. LFN study on different area devices are compared in Fig. 5. It is can be seen that LFN PSD is similar for all four devices with various areas, which is consistent with the localized current conduction model in LRS.

Fig. 3. Normalized PSD plot for (a) Fresh (b) HRS (c) LRS states under small bias. The noise PSD is independent of bias conditions for all three states.

Fig. 4. (a) Measured noise PSD of HRS state for device L10 to L100. (b) Area normalization on HRS PSD spectrum results in a similar noise level for all devices.

Fig. 5. Measured noise PSD of LRS state for device L10 to L100.
IV. CONCLUSION

Current conduction mechanism in oxide-based RRAM device has been investigated with DC measurement and LFN analysis in this work. 1/f noise behavior is observed in metal oxide based RRAM devices. Normalized noise spectrum shows no dependence on the biasing voltage, which indicates an intrinsic noise property of the current conduction. Together with DC current voltage characteristics, it is confirmed that for LRS, current conduction is localized without area dependence, whereas, for HRS, uniform leakage current scales with device area.

REFERENCES


