

A 5 V_{PP} Differential Output Swing MZI Driver Amplifier in 65 nm CMOS for Optoelectronic Applications

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Abstract—Mach Zehnder Interferometric (MZI) modulator based optical communication systems are finding increased research interests. With the rapid scaling of technology, obtaining higher output swing required for driving the MZI modulator has become increasingly challenging. To address this issue, this paper demonstrates a driver amplifier for the MZI modulator with a 5 V_{PP} differential swing in 65nm CMOS. Post layout simulation results show that for 5 Gb/s data rate, the driver consumes 308 mW from a 4 V power supply, which is significantly less power consumption compared to previously reported MZI modulator drivers. Simulation results also confirm the driver operation at 10 Gb/s.

Index Terms—Driver amplifier, fiber optic communication, MZI, optical modulator.

I. INTRODUCTION

With the growing demand for high data rates among short and medium range wired communication systems, fiber optic communication systems are rapidly replacing their electrical counterparts. Although laser diode based optical modulators are still being used widely, external modulators such as MZI have gained large interest recently because of their potential for monolithic integration with electrical circuits. Unlike laser diodes which do electrical to optical conversion, MZI modulators use waveguides to change the intensity of light passing through them based on an applied electrical potential across its length. As a result, in order to produce same extinction ratio, the driving circuit for MZI modulators should have higher voltage swing compared to laser diode drivers[1] and at the same time should also satisfy the high switching speed requirements. To achieve these specifications, MZI modulator based driver circuits employ III-V, Bi-CMOS or Si-Ge technologies leveraging their high mobility and high breakdown voltage devices [2]-[5]. However, these technologies require specialized processes, expensive packaging and assembly. Additionally, the area and power consumption of these compound processes make them less effective for commercial deployment.

Realization of such modulator driver circuit in CMOS technology would not only eliminate the need for complex post processing and packaging, but would also enable low cost and low power single chip solution. However, the scaling of device technology and consequently, reduced supply voltages make the realization of high speed and high output swing driver circuit increasingly challenging. In this paper, we developed a driver amplifier in 65nm CMOS to

produce differential output voltage swing of greater than 5

V_{PP} with a supply voltage of 4 V. The driver incorporates a drain-gate feedback network that allows usage of regular and thick gate MOS devices to achieve data rates as high as 10 Gb/s.

Section 2 provides a system overview of the MZI modulator based driver IC along with its design requirements. Section 3 describes the circuit design of pre-driver and driver amplifier with the drain-gate feedback network. The schematic level and post layout simulation results are presented in Section 4, followed by conclusion in Section 5.

II. SYSTEM OVERVIEW

Fig. 1 shows the MZI modulator based transmitter for optoelectronic communications. The transmitter converts high speed electrical input data into an optical signal with the help of a driver amplifier and an optical modulator (MZI). The MZI consists of two arms, and operates on the principle of electro-optic effect such that the light passed through the two arms is phase shifted due to the free carrier dispersion induced by the electric potential applied to the modulator substrate of each branch [5]. Since the two arms are differentially excited, when the light passing through them is combined, it undergoes constructive or destructive interference to obtain intensity modulated optical output. The MZI arms which are typically 4 mm long require electric fields of the order of several volts to generate the required phase shift along the optical path. To achieve 5 Gb/s operation with sufficient extinction ratios of 6 – 10 dB, the MZI modulator needs a peak to peak differential voltage swing of greater than 5V at its input. This is achieved by a high voltage swing driver designed in this work as shown in Fig. 1.

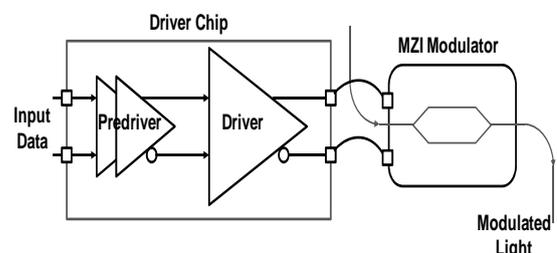


Fig. 1. Driver IC and MZI modulator system architecture.

A two stage predriver operating at 1.2V supply generates the necessary input swing required by the main driver circuit. Although single chip integration of the modulator and the driver has already been reported [5], they use specialized silicon on insulator (SOI) process to accommodate the driver

and the modulator on the same chip. To avoid process complexity and expensive packaging, we developed the driver IC on a separate chip that can be directly wire bonded to the MZI chip while both the driver IC and the modulator chip are mounted on a PCB.

III. HIGH OUTPUT SWING DRIVER DESIGN

Generating output voltage swing of $5 V_{pp}$ at 5 Gb/s poses several challenges in designing the driver circuit in a deep submicron CMOS process with a supply voltage of 1.2 V. Firstly, scaled supply voltages in deep submicron technologies and smaller breakdown voltages of the transistors limit the voltage headroom to 1V. Secondly, large RC parasitics in the MZI severely restrict the speed of operation to few Gbit/s. Although some circuit techniques such as breakdown voltage doubler circuit have reported output voltage swings as high as 2-3 times that of the supply voltage, they either rely on Bi-CMOS or III-V processes to increase the output swing [2]-[4], or their speed of operation is limited to few hundred Mbit/s [6]. To overcome these difficulties while maintaining the high speed of operation, the driver developed in this paper utilizes drain-gate capacitance feedback network [8] to achieve higher output swing.

Fig. 2 shows the schematic of the predriver and driver circuits. The two stage differential predriver employs current mode logic (CML) with a supply voltage of 1.2 V. The main function of the predriver is to provide impedance matching and to feed the main driver with a constant swing at its input.

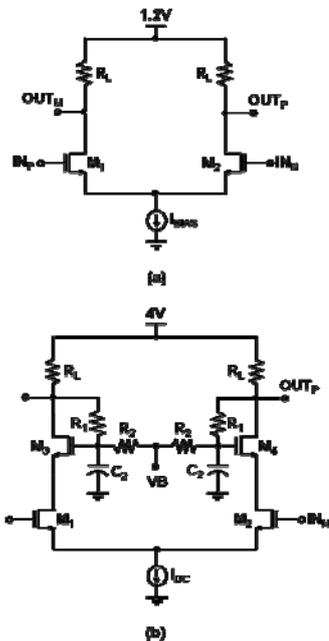


Fig. 2. Circuit schematic of (a) Predriver (b) Main driver Amplifier

The first stage of the predriver is connected to an off-chip impedance matching network in order to match the input impedance to the 50Ω source impedance of the data generator. The second stage drives the high impedance input of the main driver while maintaining constant swing and common mode voltage at its output. This is achieved by varying the tail current and changing the digitally controlled load resistance in the differential pair.

The main driver circuit uses differential cascode topology

with 4 V supply voltage and incorporates drain-gate capacitance feedback to share the high output swing between the cascode transistors. Transistors M_1 and M_2 are regular fast switching thin oxide NMOS transistors with breakdown voltage of 1.2 V, while the cascode pair M_3, M_4 are thick gate devices that can tolerate 3.3 V across their terminals. The drain-gate feedback network consists of resistors R_1, R_2 and capacitor C_2 . Resistors R_1 and R_2 form the DC feedback path, while the capacitor C_2 and drain gate capacitance C_{gd} of M_3 and M_4 form the high frequency feedback path between the output and the gate of M_3 and M_4 devices. This configuration ensures that a part of the output is fed back to the gate so that the output voltage is divided across the two cascode transistors instead of just the thick gate device when the feedback network is not used. Since the high frequency feedback component is critical in determining the output voltage swing and speed of operation in the circuit, 3-bit programmability is added to capacitor C_2 in order to mitigate the effects of process and temperature variation. The value of resistors R_1, R_2 and voltage V_B is chosen such that DC feedback is maintained at an appropriate level and the voltages across any two terminals of M_3 and M_4 do not exceed their breakdown voltage.

The MZI modulator load was estimated to be 45Ω with a capacitance of 150 fF. The load resistance R_L of the driver is therefore selected as 50Ω to match with the MZI as well as with the 50Ω SMA cables for testing purpose. The tail current source draws a constant current of 70 mA to charge and discharge the capacitive MZI load at 5 Gb/s.

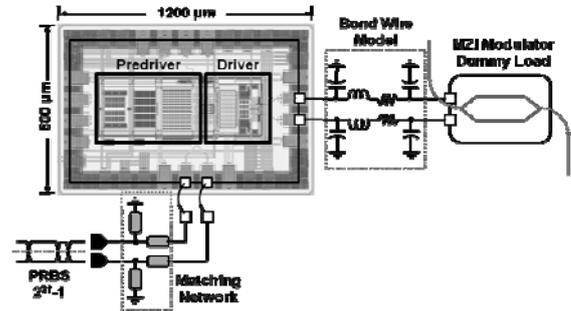


Fig. 3. Chip layout with post layout simulation setup.

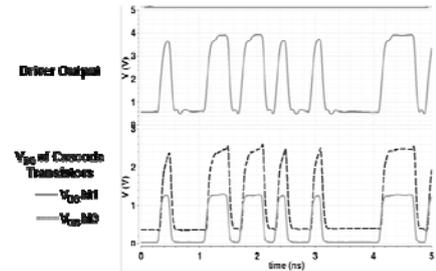
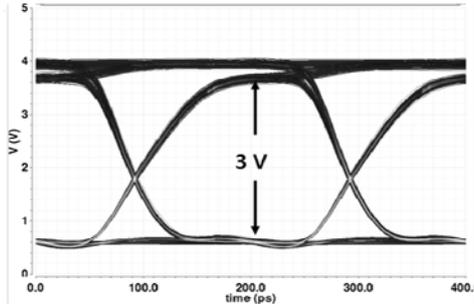


Fig. 4. Post layout transient simulation results of the proposed driver IC at 5 Gb/s

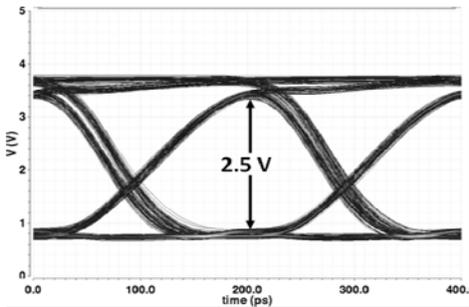
IV. SIMULATION RESULTS

As the driver chip would be connected to the external PCB through bond wires, an equivalent circuit model of the bond wires as shown in Fig. 3 was added at each input and output pad in the post layout simulation setup. S-parameter response of the MZI modulator was used as a load for the driver to emulate actual testing conditions. An input matching network was inserted between the data source and the differential

input pads of the driver chip to match the source and cable impedance. A $2^{31}-1$ PRBS waveform with magnitude of 600 mVPP and data rate of 5 Gb/s was input to the predriver. Transient post layout simulation results in Fig. 4 demonstrate the driver operation. Transistors M_1 and M_3 share the output swing to generate single ended peak-to-peak output swing of 2.5 V. Simulation results further confirmed that none of the devices exceeded the breakdown voltage limit.



(a)



(b)

Fig. 5. Transient eye diagram of the proposed driver IC at 5 Gb/s (a) Pre-layout simulation (b) Post-layout simulation.

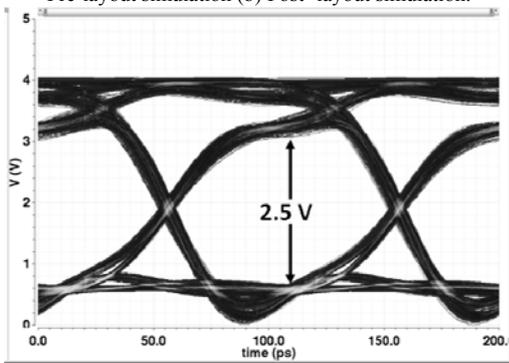


Fig. 6. Simulated transient eye diagram of the proposed driver IC at 10 Gb/s.

Fig. 5(a) and 5 (b) depict the eye diagram of schematic level and post layout simulation with an eye opening of 3 V and 2.5 V, respectively. When converted to power levels equivalent to a 50 Ω resistor, this voltage swing corresponds to an extinction ratio of greater than 7 dB which is sufficient to drive the MZI modulator. The functionality of the driver IC was further verified for data rate of 10 Gb/s. As depicted in Fig. 6, the pre-layout simulation results showed a good eye opening with the single ended output swing as high as 2.5 VPP. The data rate can be further improved by introducing bandwidth enhancing techniques such as inductive peaking at the cost of additional area, or by replacing the thick gate

cascode device with a regular high speed 1.2V device at the cost of reduced output swing.

From the post layout simulation results, the driver consumed 68mA from a 4 V supply, while the predriver consumed 30 mA from 1.2 V supply at 5 Gb/s. This corresponds to a total power consumption of 308 mW, which is significantly less than that reported in recent similar works. Table I summarizes the performance of the driver IC.

TABLE I: PERFORMANCE SUMMARY OF THE DRIVER IC

Technology	65 nm CMOS
Supply Voltage (V)	4
Die Area (mm ²)	0.96
Data Rate (Gbit/s)	5
Single Ended Output Swing (VPP)	2.5
Extinction Ratio (dB)	7
Power (W)	0.308

V. CONCLUSION

A high output swing driver amplifier for MZI modulator is proposed in this paper for high speed optical communication links. By incorporating thick gate cascode devices and a drain-gate capacitive feedback, the differential output swing of 5 VPP was obtained. Post layout simulation results confirmed the driver operation at the data rate of 5 Gb/s. With the usage of regular 65nm cascode transistors and the reduction in parasitic by improved layout, the driver speed can be increased beyond 10 Gb/s.

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