

Low Noise Low Power Preamplifier for Integrated Ultrasound Needle Intervention Application

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Abstract—This paper presents the design and implementation of a fully integrated trans-impedance amplifier (TIA) as the pre-amplifier of analog front-end for ultrasound needle intervention application. The application demands very low power solution for the receiver operating in the frequency band 1.3 MHz to 3.9 MHz. The design adapts low power architecture to create low noise electronic interface for Capacitive Micro-machined Ultrasound Transducers (CMUT) sensor. Using a 0.18- μm CMOS/DMOS process, simulation results of this interface IC show that the proposed TIA can provide 104 dB trans-impedance gain, 1.44 nArms input referred noise integrated over frequency band 1.3 MHz to 3.9 MHz, while consuming 200 μA current from 1.8-V supply.

Index Terms—Analog front-end, capacitive micro-machined ultrasound transducer, trans-impedance amplifier.

I. INTRODUCTION

Ultrasonic needle intervention shows tremendous potential in enhancing safety and confidence level in many diagnostic procedures like amniocentesis, chorionic villus sampling, epidural anaesthesia, liver biopsy etc [1]. In this approach an ultrasonic trans-receiver embedded in the intervening needle provides the real time image of the internal organs thereby providing greater feedback and control over the needle, leading to better safety for the procedure. The system comprises of a 1-dimensional (1D) capacitive Micro-machined Ultrasound Transducer (CMUT) array, supporting front-end circuit and portable image display that provides real-time ultrasound images as shown in Fig.1.

The associated trans-receiver architecture for this application is shown in Fig.2. It includes a transmit path and a receive path. The receiver consists of a preamplifier and a time gain compensator (TGC) that compensates for signal attenuation as function of depth. The TGC is implemented by a variable gain amplifier (VGA) where a time varying control signal is applied to the VGA gain control input such that the signal strength at the VGA output is constant over time. The TGC is followed by low pass filter (LPF), analog-to-digital converter (ADC) and image processor to generate real-time image. The transmitter chain consists of a pulse generator, a programmable delay block, and a transmit driver to drive the transducer.

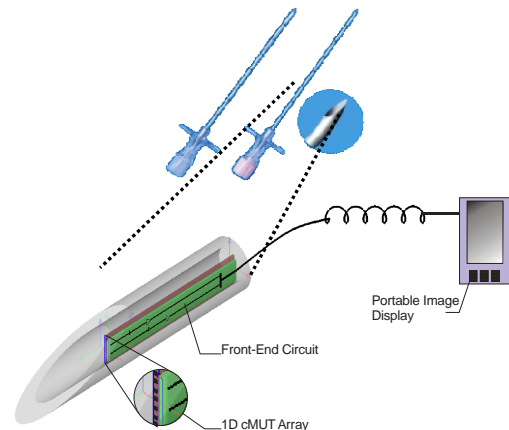


Fig. 1. Schematic illustration of ultrasound needle

The pulse generator produces 10-V pulse in the frequency range of interest to the transducers through programmable delay chains to enable electronic beam focusing. A transmitter/receiver switch is placed in between the transducer and the transceiver IC in order to control the transmit/receive mode and also to protect the receiver from the high transmit voltage pulses used to excite the transducer array. Multiple trans-receiver channels and transducers are required for ensuring desired image quality. Owing to the real-time operation of the front-end circuitry inside the patient's body, the application demands very low power budget from the analog front-end. Also the requirement to fit the entire system inside the needle sets very stringent requirement on chip area.

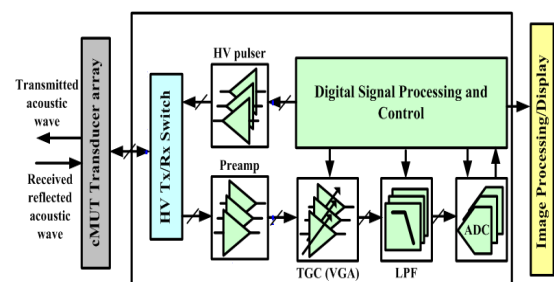


Fig. 2. System diagram of ultrasound imaging system

Due to high electrical impedance of CMUT devices, wide-band current amplification is required at the pre-amplifier stage. Trans-impedance amplifier (TIA), owing to its low input impedance has been a preferred choice in this case. So far different TIA topologies have been used by researchers for ultrasound preamplifier application [2-6]. Among all the topologies reported cascaded common-source, source-follower structure with resistive feedback appears to be the most common choice due to its obvious merits [2-4]. In this paper, we have analyzed that resistive feedback around

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an inverter can serve as even better candidate for achieving low power budget while satisfying the performance required for this application. The simulation result shows that this design can achieve more than 100 dB trans-impedance gain, 1.44 nArms integrated input current noise over the frequency band of 1.3 MHz to 3.9 MHz while consuming around 200 μ A current from a 1.8-V supply. The rest of the paper is organized in the following manner. Section 2 justifies the suitability of this topology as compared to traditional cascaded common-source, source-follower structure through small signal analysis. Section 3 reveals the circuit design following discussion about specification. Section 4 shows post-layout simulation result covering relevant design metrics. Section 5 concludes the paper.

II. CIRCUIT ANALYSIS

The core amplifier, that we are going to use as preamplifier, is essentially an inverter. The shunt-shunt feedback around it through a resistor makes it suitable to serve as a good trans-impedance amplifier. In order to judge the suitability of this topology as TIA we are going to compare key design parameters of this architecture with the traditional TIA topology (cascaded common-source and source-follower topology) on the basis of small signal analysis. Fig. 3 shows the two topologies stripped to their basics.

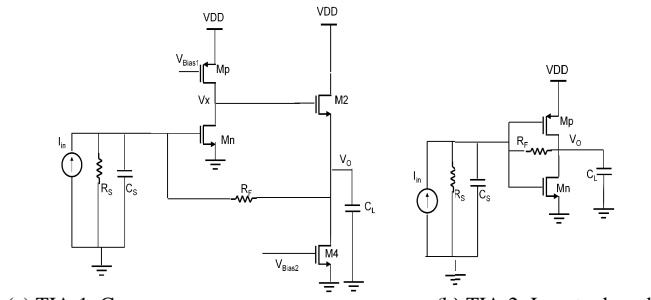


Fig. 3. TIA Topologies

Equation (1) shows TIA-1 trans-impedance dc gain.

$$\frac{V_o}{I_{in}} = \frac{\frac{1}{gm_2} - R_F A_{v1}}{A_{v1} + \frac{1}{A_{v2}}} \approx \frac{-R_F}{1 + \frac{1}{A_{v1} A_{v2}}} \quad (1)$$

A_{v1} and A_{v2} are intrinsic voltage gains of common-source stage and source follower stage respectively, as described in (2) and (3) below. Here gm and gds represent transconductance and output conductance of respective MOS respectively. R_F is the feedback resistor as shown in Fig. 3.

$$A_{v1} = \frac{gm_n}{gds_n + gds_p} \quad (2)$$

$$A_{v2} = \frac{gm_2}{gds_2 + gds_4 + gm_2} \quad (3)$$

Trans-impedance from (1) shows that trans-conductance of the source follower transistor M2 should be large enough to satisfy $gm_2^{-1} \ll R_F A_{v1}$. Also the source follower voltage gain being less than unity the trans-impedance gain becomes lower than that of a single stage one. However, trans-impedance dc gain (4-5) of inverter based topology can achieve higher value owing to higher equivalent gm and higher intrinsic voltage gain A_v under same current consumption.

$$\frac{V_o}{I_{in}} = \frac{\frac{1}{gm_{eq}} - R_F}{1 + \frac{1}{A_v}} \approx \frac{-R_F}{1 + \frac{1}{A_v}} \quad (4)$$

$$A_v = gm_{eq} * ro_{eq}, gm_{eq} = gm_n + gm_p, ro_{eq} = \frac{1}{gds_n + gds_p} \quad (5)$$

In terms of output impedance also this topology shows better promise because of higher voltage gain at same power consumption. Equations (6) and (7) show the output resistance of TIA-1 and TIA-2 respectively.

$$R_{out} = \frac{(\frac{1}{gm_2} \parallel \frac{1}{gds_2} \parallel \frac{1}{gds_4})}{1 + A_{v1} A_{v2}} \quad (6)$$

$$R_{out} = \frac{1}{gm_{eq} + ro_{eq}^{-1}} = \frac{ro_{eq}}{1 + A_v} \quad (7)$$

For a given trans-impedance gain (decided by specification) only core amplifier noise can be reduced. In case of TIA-1 noise from source follower stage also contributes to the overall amplifier noise, thereby resulting in higher overall input referred noise, as derived in (8), than that of TIA-2, shown in (9).

$$\tilde{I}_{in,n}^2 = \left(\frac{4KT\gamma}{R_F^2} \right) \left((gm_p + gm_n) \frac{1}{gm_n^2} + \frac{1}{A_{v1}^2 gm_2^2} (gm_2 + gm_4) \right) + \frac{4KT}{R_F} \quad (8)$$

$$\tilde{I}_{in,n}^2 = \frac{4KT\gamma gm_{eq}}{R_F^2 gm_n gm_p} + \frac{4KT}{R_F} \quad (9)$$

Here γ is a parameter associated with thermal noise of MOS device. The frequency response of TIA-1 also imposes some critical problems. Other than the two poles associated with input and output node the device capacitance associated with node X offers an extra pole. With three poles around the feedback loop this TIA can even oscillate. On the other hand, in case of TIA-2 there are only two poles associated with input and output node. As a result, stability can be easily assured. The equation (10) captures the trans-impedance frequency response for TIA-2.

$$\frac{V_o}{I_{in}} = \frac{(R_F C_F s + 1 - g_{m_{eq}} R_F) r_{o_{eq}}}{R_F r_{o_{eq}} \alpha^2 + [R_F (1 + A_v) C_F + r_{o_{eq}} C_L + R_n (1 + A_v) C_{in}] s + (1 + A_v)} \quad (10)$$

where

$$R_{in} = \frac{R_F + r_{o_{eq}}}{1 + A_v}, \quad \alpha = C_F C_L + C_L C_{in} + C_F C_{in} \quad (11)$$

C_F accounts for gate to drain capacitance of two MOSFETs along with parasitic cap associated with the feedback resistor. Interestingly, this structure introduces one RHP zero at

$$\omega_z \approx \frac{g_{m_{eq}}}{C_F}. \text{ However, this zero falls at a very higher}$$

frequency compared to our frequency of interest.

III. CIRCUIT DESIGN

First the specification was derived through careful system design. The required trans-impedance gain is 100 dB over a frequency band 1.3-3.9 MHz, while keeping the integrated input referred current noise within 3 nArms. The design has to provide a wide dynamic range in order to support input current signal amplitude in the range 14.5 nA to 4.55 μ A. The load offered by next stage is RC parallel load - 250K || 150fF. The desired power consumption has to keep within 400 μ watt from a 1.8V supply. The CMUT device at the input to the TIA is modeled as shown in Fig.4. It is an AC current source in parallel with the intrinsic source impedance of the CMUT. Fig.5 shows the preamplifier circuit. In order to make the amplifier insensitive to power supply it is wise to bias it with a current bias. However, in the whole system the TIA power will be supplied from a LDO. This will obviate the need to bias it through a current source.

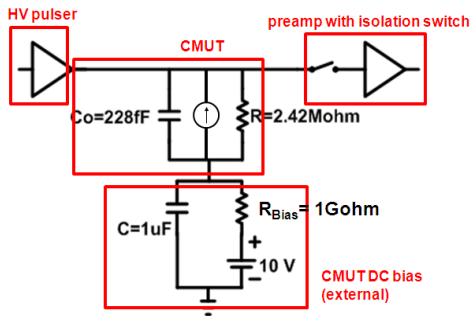


Fig. 4. CMUT model

As per discussion in section II, feedback resistor R_F needs to be more than 100 K to satisfy trans-impedance gain of 100 dB. Ignoring flicker noise, we figured out g_m needed for the input transistors to meet the noise criteria from (9). This allows us to choose a bias current for the amplifier stage. Approaching this way, the device sizes are optimized to meet other design metrics. Special care is taken during layout to reduce parasitic cap associated with feedback resistor R_F . In order to relax dynamic range requirement of later stages we

add 20 dB of coarse grain-tunability through switches in the resistive feedback path. At lower gain settings the inverter bias current is reduced accordingly, since at higher input signal the amplifier can afford to have larger noise. This way some power can be saved at lower gain mode. The capacitor C_b is used to bypass the noise from bias current. The T/R switch is implemented with 30-V NMOS device so that it can sustain 10-V pulses during transmit mode. RX_EN is used to turn off the preamplifier during transmit mode.

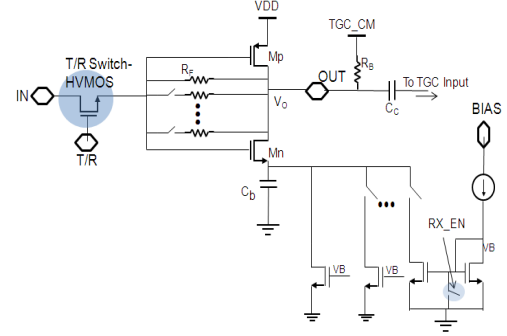


Fig. 5. Inverter based TIA

IV. POST LAY-OUT SIMULATION RESULT

The design has been carried out using Global foundry 0.18- μ m CMOS/DMOS 1P6M PDK. All circuit simulations are done with Cadence-Spectre simulator. Fig. 6 shows the final layout of the proposed circuit. During simulation the board and package parasitic have been considered.

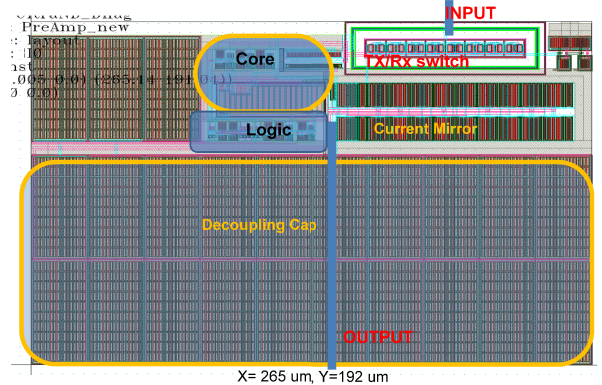


Fig. 6. Preamplifier layout

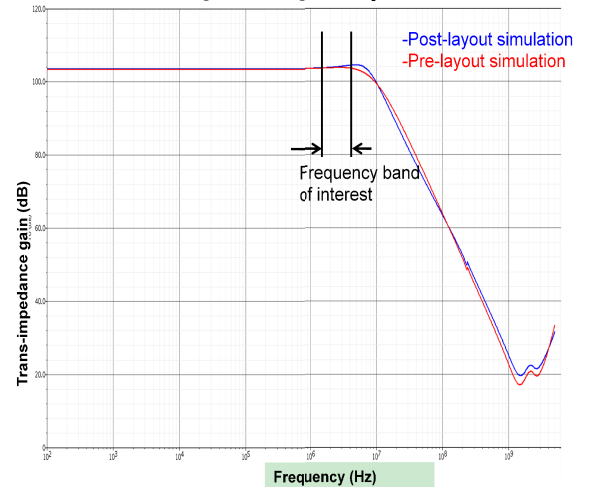


Fig. 7. Trans-impedance frequency response

Fig.7 captures trans-impedance gain frequency response for both pre-layout and post-layout simulation at maximum

gain setting. Around 104 dB trans-impedance gain has been achieved over the bandwidth of 1.3 MHz to 3.9 MHz. Fig.8 shows the input referred noise power density plot for both pre-layout and post-layout simulation at maximum gain setting. The integrated input referred noise calculated over frequency band of interest is 1.44 nArms for post-layout simulation.

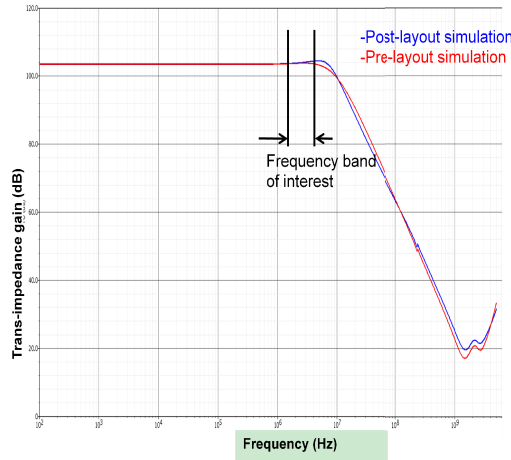


Fig. 8. Trans-impedance frequency response

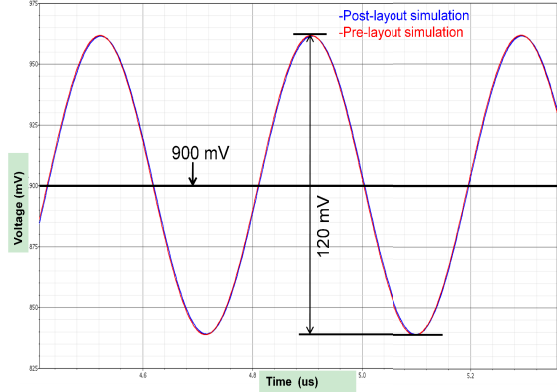


Fig. 9. Transient simulation under 9.1 μ A peak-to-peak input current swing

Fig. 9 demonstrates the TIA output for maximum input current swing i.e. 9.1 μ A peak-to-peak. For maximum input swing case the circuit is operated at minimum gain mode.

This simulation with largest signal swing ensures that there is no visible distortion or any sign of ringing. The circuit consumes only 200 μ A current from 1.8-V supply qualifying it an ideal candidate for needle application.

V. CONCLUSION

We present the design and implementation of a fully integrated front-end preamplifier dedicated to interface 1D CMUT array for ultrasonic needle applications, using 0.18- μ m CMOS/DMOS 30-V HV fabrication technology from Global Foundries. New fully integrated low power low noise preamplifier has been described. Simulation results validate its ability to meet the specifications of ultrasonic application. The proposed circuit has been sent for fabrication and measurements will be done when the prototypes are ready.

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