

A Low Power Image Sensor Controller and JPEG Encoder IC for Wireless Capsule Endoscopy

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Abstract—In this paper, a low power CMOS image sensor controller and baseline JPEG compression encoder for wireless capsule endoscopy is presented. The proposed JPEG encoder can be integrated into a wireless capsule system to compresses the raster YCbCr 4:2:2 raw image data from image sensor into JPEG format file and then send to external receiver through wireless transmission. To achieve low power and high image compression ratio, the JPEG compression algorithm is optimized for biomedical image compression. The compressed image data are being packed into byte format and DMA can be used to retrieve the JPEG image. The JPEG image compression chip is designed using 0.18- μm CMOS technology. It consumes 1.69 mW under 6 MHz system clock for VGA (640 \times 480) image resolution when compressing at 7.5 frames per second.

Index Terms—Discrete cosine transform (DCT), direct memory access (DMA), huffman coding, JPEG, image compression.

I. INTRODUCTION

Wireless capsule endoscopy (WCE) has received increasing attention in recent years as it is a safe and efficient emerging technique to provide endoscopic examination of the gastrointestinal tract, especially the small intestine, which is difficult to check with other types of conventional endoscopy [1]. It has been proven that WCE is able to provide useful information for small intestine bleeding and tumor diagnosis which are the major reasons for gastrointestinal diseases [2]-[4]. In 2001, the usage of WCE was first approved by the U.S. food and drug administration (FDA) and since then different types of WCE have been developed around the world [5].

A typical WCE consists of a miniaturized camera with illumination source, a wireless transmitter for image data transmission and battery module to power the whole system. Fig. 1 illustrates a typical application scenario of wireless capsule endoscopy. The captured image data are transmitted through the wireless link to the external portable personal healthcare server which can be installed in a personal digital assistant or smart phone. The received images are then forwarded to the doctor through internet for diagnostic and therapeutic purposes. After the patient swallows a WCE, it

will move through the gastrointestinal tract naturally with the aid of the peristaltic movement of the intestine. The patient will not feel uncomfortable during the whole process because the capsule size is similar to a vitamin pill and easy to swallow, the disposable capsule can be expelled out normally.

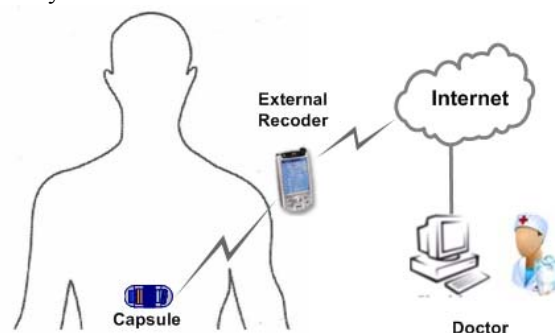


Fig. 1. The application scenario of wireless capsule endoscopy.

The major performance specifications of a WCE include image resolution, image frame rate and system power consumption. Current commercial WCE adopts QVGA (320 \times 240) resolution and its one-way telemetry from capsule to base station (BS) can only transmit low-resolution images at low frame rate (2 fps). To facilitate accurate diagnosis, high-resolution video-quality image is preferred by doctors. However the performance improvement is limited by the power budget since the battery capacity is limited by the capsule size constrain and the system is required to work continuously 8-10 hours during its stay in the human body.

Low-power image compression is potentially a key technology for high-resolution, high frame rate image transmission [6]. It can relax the requirements on processing speed of transmitter baseband and spectrum bandwidth of RF TX significantly, so that the system power consumption can be greatly reduced. Dedicated image encoders for WCE have been reported in literature [7], [8]. The trade-off among power consumption, compression ratio, and image quality is the major design challenge.

In this paper, a single chip low power image compressor, targeting for wireless ingestible capsule applications is proposed. It employs compression ratio higher than 15:1 while maintaining the quality of biomedical images. By exploiting the quality factor and compression ratio, some techniques are proposed to lower the computation complexity, which helps reduce the latency, power and area compared to conventional implementation.

This paper is divided into four sections. Section II gives an overview of the image compression algorithm. Section III presents the hardware implementation. The implementation results and performance of this work are presented in section

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IV, the conclusions are made in section V.

II. OVERVIEW OF JPEG IMAGE COMPRESSION

There are two types of image compression methods, namely lossless and lossy. For lossless method, the exact original image can be reconstructed after compression and decompression. On the other hand, for lossy method, the reconstructed image only gives closed approximation to the original image. Standard lossless image compression formats such as bitmap (BMP), graphics interchange format (GIF), portable network graphics (PNG) and tagged image file format (TIFF) have a compression ratio of around 3:1 or less. Lossy image compression formats, such as joint photographic experts group (JPEG) and JPEG2000, have a scalable compression ratio which can trade off with image quality. Baseline JPEG and JPEG2000 employ discrete cosine transform (DCT) and wavelet transform respectively. JPEG algorithm is less computational intensive. Furthermore, the deterioration in image quality is slight at compression ratio less than 20:1. Therefore, JPEG compression is generally preferred when simplicity and computational cost are important considerations.

A generic JPEG compression block consists of 3 major operations steps, including 2-dimensional (2-D) discrete cosine transformation (DCT), quantization and entropy encoding as shown in Fig. 2. The 2-D DCT operation transforms a fixed size matrix size of image data from its spatial domain to frequency domain. For general non-computer graphic images, higher frequency components tend to have lower value than lower frequency components. Quantization operation further reduces the coefficients of DCT especially on the high frequency components which are likely to become zero. Higher compression ratio can be achieved by trading image quality with the use of larger quantization values. Entropy encoding is a lossless operation. Typical JPEG compression entropy encoder is the Huffman encoder. The DC coefficient will be differential pulse code modulated (DPCM) prior to Huffman encoding. AC coefficients will be arranged in low to high frequencies, which will be in zigzag manner, and then Huffman encoded with zero-run length encoding.

III. HARDWARE IMPLEMENTATION

Commercial image sensor is usually controlled and initialized via the standard 2-wired serial interface I2C. The image sensor is a slave device with 7-bit serial bus slave address. The image sensor can be configured by writing the parameter registers via I2C. The frame rate of the image sensor is control by the master clock instead of using the build-in clock divider in the image sensor. I2C master is implemented in the image sensor controller to send out a set of write command, as shown in Fig. 3. The data, needed to be written to the parameter registers in the image sensor, is stored in a read-only memory (ROM). The I2C master controller will fetch the data from the ROM and send to the image sensor upon system power up and system reset. The full chip JPEG compression architecture is shown in Fig. 4. It is pipelined into 6 stages. The first stage is the input buffers,

second to fourth stages are the JPEG compression algorithm core, data packer is in the fifth stage and the last stage is the buffer.

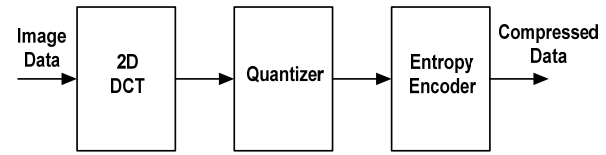


Fig. 2. The generic JPEG compression signal flow.

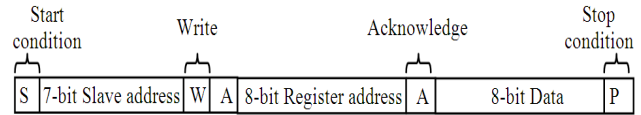


Fig. 3. The data format of I2C write command.

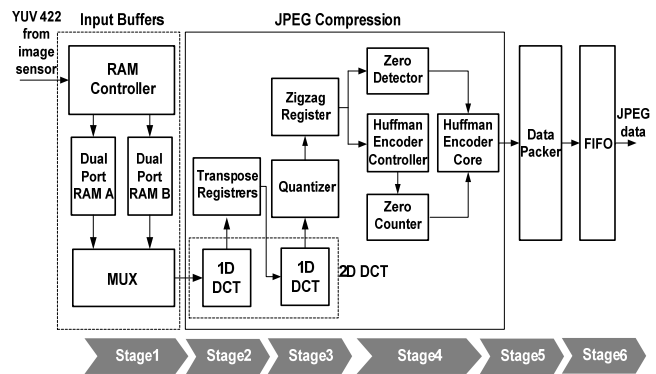


Fig. 4. Image compression block diagram.

In stage 1, the input buffers store 16 rows of image data. The random access memories (RAM) are divided into 2 blocks, each storing 8 rows of image data in read and write ping-pong scheme. The JPEG compression core is pipelined into 3 stages and the 2-D DCT is pipelined into 2 stages. Stage 2 consists of 1D-DCT and the transpose / pipeline registers. Stage 3 includes the fast 1D-DCT as well as the quantizer and the zigzag / pipeline registers. Quantization operation is performed right after the second DCT operation without any pipelining. The JPEG quality factor is fixed, thus the luminance and the chrominance quantization values are known. Instead of doing division directly, the quantization values are being multiplicative inversed. After quantization, the data will be of smaller value, thus the zigzag registers, which is used to arrange the coefficients from low to high frequencies, can have lesser data width. The whole stage 4 is doing the DPCM for DC coefficient, zero-run-length encoding for AC coefficients and Huffman encoding. Zero counter is used for zero-run-length encoding while the zero detector is used for end of block encoding. Static compression technique and standard JPEG Huffman codes are employed. Stage 5 is the data packer which organizes the variable length output of the JPEG compression into 8-bit data format. The data packer consists of a FIFO and a controller which sends out 8-bit data and the data clock whenever 8-bit of data is available. Stage 6 is particularly uses for DMA interface. It consists of a FIFO and a controller. Its' write operation is performed by the data packer and read operation is performed by the device interfaced with the full chip JPEG compression. The controller also sends out signal to inform the external device about the status of the FIFO so as to prevent overflow or underflow condition.

TABLE I SUMMARY OF PERFORMANCE AND COMPARISON WITH STATE-OF-ARTS

Specifications	[7]	[8]	[9]	This Work
Color Plane	RGB	RGB	YUV422	YUV422
Compression Type	JPEG-LS	H.264	DPCM	JPEG
Image size	640×480	512×512	256×256	640×480
Clock Rate	20M	4M	NA	6M
Frame Rate (fps)	2	2	2	7.5
Compression Ratio	2	5.6	4.1	15.6
PSNR (average)	46.4	36.2	43.6	44.56
DC power (mW)	1.3	0.92	0.73	1.67
Process	0.18 μm	0.18 μm	0.18 μm	0.18 μm

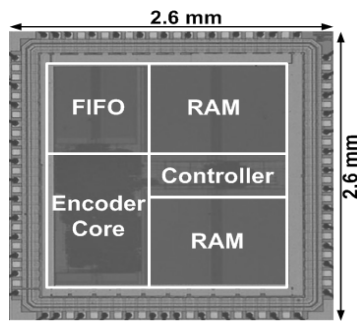


Fig. 6. Chip photo of JPEG encoder.

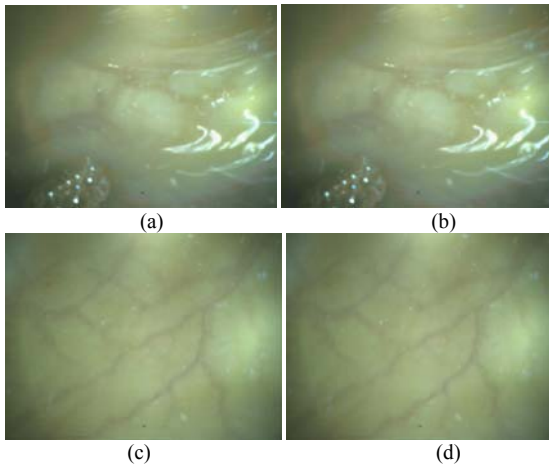


Fig. 7. Bayer RGB (a) (c) and JPEG compressed images. (b) (d)

IV. MEASUREMENT RESULTS

The image sensor controller and the full chip JPEG compression is fabricated in 0.18 μm CMOS technology and has a die area of 2.6 mm \times 2.6 mm as shown in Fig. 6. Pixelplus image sensor is used to verify the functionality of the chip and a FPGA is employed for DMA reading. The Pixelplus image sensor has 776 \times 516 pixels and it is initialized to output YCbCr 4:2:2 images and master clock of 6 MHz is generated for the image sensor to run at targeted 7.5 fps. The full JPEG compression chip consumes only 1.69 mW at 7.5 fps using 1.2 V operating voltage.

The PSNR and compression ratio are evaluated by setting the image sensor to output bayer RGB data. After capturing the Bayer RGB data, conversion to YCbCr 4:2:2 format was done prior sending it into the JPEG compression chip. The conversion is achieved with Verilog coding and FPGA to mimic the image sensor function. The captured bayer RGB

images and the JPEG compressed images are illustrated in Fig. 7. For endoscopy images, the typical PSNR is around 42 dB and compression ratio of 13-15. The performance of the JPEG compression ASIC is summarized in Tab. I and compared with other state-of-arts. It can be observed that this design outperforms in terms of compression ratio and frame rate with minor power consumption overhead.

V. CONCLUSIONS

An integrated single chip CMOS image sensor controller and JPEG encoder for wireless capsule endoscopy is presented in this paper. With the image sensor controller, capturing and compressing of different resolution images can be achieved. Implemented in 0.18- μm CMOS process, the JPEG compression chip employs interleaving baseline JPEG image compression method with quality factor of 90 and achieved more than the targeted compression ratio of 15:1. It can be employed in applications which require image sensor control and direct interface with image sensor and DMA.

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