Reconfigurable Closed-Loop Digital ΔΣ Capacitive MEMS Accelerometer for Wide Dynamic Range, High Linearity Applications

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Abstract—**Closed-loop capacitive MEMS accelerometer is similar to a ΔΣ ADC where the MEMS sensor introduces second-order dynamics in the loop. The sensor has limited signal gain, hence provides very limited noise shaping capability to other noise contributions within the loop. Furthermore, fabrication non-idealities can cause unwanted stability issues in higher order closed-loop operation. We present a 4th order ΔΣ closed-loop system with a digital 2nd order ΔΣ modulator. The digital ΔΣ modulator allows fine accuracy in choosing the coefficients for the ΔΣ modulators. It also provides flexibility in the placement of poles and zeros for compensating the unforeseen phase delays caused by fabrication non-idealities. Our system is able to achieve an SNR > 120dB in simulation and > 90dB from experiment with an evaluation board. The digital implementation of ΔΣ modulator allows us to build reconfigurable closed-loop system with the potential for even higher order system which can be optimized to suit different MEMS sensor characteristics and performance.**

Index Terms—**Noise transfer function, electronic filter, feedback, MEMS sensor**

I. INTRODUCTION

Capacitive MEMS accelerometers with opened-loop readout architecture have demonstrated high performance capabilities with very large dynamic range (>120 dB) [1]. The analog front-end (AFE) of the readout circuit consists of a low-noise preamplifier with large gain to reduce the noise contribution of the subsequent signal conditioning circuits. These accelerometers are found in many applications from automotive to medical [2] where high resolution and/or wide dynamic range are required. Opened-loop architecture is not suitable for navigation applications where high linearity (<0.01%) is also important. The linearity limitation comes from the MEMS sensor itself. The capacitive sensors have output responses that are inversely proportional to their plate/finger distance. Therefore, for large acceleration sensing, the output response becomes highly non-linear.

Closed-loop operation corrects the non-linearity problem using force feedback. The feedback force balances the sensor structure around its nominal position through electrostatic feedback. Thus, the feedback force becomes a measure of the externally applied force with high linearity.

Electrostatic feedback can be implemented as variable voltage feedback (analog) or constant voltage bit-stream feedback (digital). The latter with a one-bit quantizer has the advantage in terms of linearity as one bit DAC is inherently linear. With digital feedback, quantization noise becomes a major noise source in the system. Quantization noise can be reduced using multi-bit feedback system [3], but at the expense of lower linearity for the closed-loop system.

Conventional approaches use a 2nd order ΔΣ loop with the MEMS sensor determining the loop dynamics [4]. The sensor has very limited signal gain providing only signal translation from acceleration to voltage output, hence it does not provide much noise shaping of the quantization noise. To achieve large SNR, higher order loop design plus oversampling is preferable. Higher loop order design is achieved by inserting an electronic filter to provide additional modulators between the AFE and the quantizer [5]. The electronic filter has high gain in the signal band and rejects out-of-band noise. Consequently, the in-band signal is amplified and the SNR is improved at the output of the quantizer. However, the electronic filter will increase the overall loop order and may cause issues in loop stability because additional poles and zeros are introduced into loop. As gain coefficients of the electronic filter affect the poles and zeros locations, optimum values for these coefficients is essential to ensure closed-loop system stability while maintaining high MEMS performance in terms of dynamic range and linearity.

In this paper, we propose high order closed-loop system architecture for wide dynamic range and high linearity MEMS accelerometers. To reduce the overall noise in the closed-loop system, an electronic filter in the form of digital ΔΣ modulators is adopted to perform noise shaping for the quantization noise. The proposed digital ΔΣ modulation architecture offers good flexibility and reconfigurability to enable fine-tuning of the gain coefficients and optimum positioning for the poles and zeros to optimize performance in term of MEMS accelerometer resolution and closed-loop system stability. Section II discusses the background of closed-loop ΔΣ MEMS accelerometer and performance issues. The proposed high order closed-loop system architecture is presented in Section III. Simulation and experiment results are presented and discussed in Section IV and V, respectively. Finally, conclusions are given in Section VI.

II. BACKGROUND

A. Closed-Loop ΔΣ MEMS Accelerometer

Fig. 1 is the top level block diagram of a closed-loop ΔΣ

MEMs accelerometer. F_{ex} is the external force applied on the MEMS sensor, T_d is the MEMS transfer function which translate input resultant force to an equivalent displacement, k_{xcv} is the equivalent signal gain from sensor displacement to equivalent input voltage V_{in}, E_n is the input referred noise for the AFE, k_{afe} is the AFE gain, H_c is the electronic filter transfer function, k_Q is the quantizer gain, Q_n is the quantizer noise, f_b is the feedback gain and F_{fb} is the equivalent force feedback to the MEMS sensor. The closed-loop system equation can be written as:
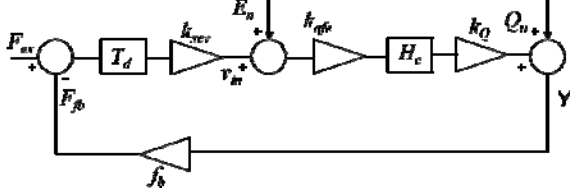

Fig. 1. Top level block diagram of a closed-loop ΔΣ MEMS Accelerometer.

$$Y = STF \cdot F_{ex} + NTF_{E_n} \cdot E_n + NTF_{Qn} \cdot Q_n \qquad (1)$$

where the output *Y* (one-bit bitstream), consisting of a sum of components made up of *STF* the signal transfer function; NTF_{En} and NTF_{Qn} which represent of the equivalent input noise transfer functions for the AFE and the one-bit quantizer respectively. From Fig. 1, *STF* can be deduced and shown as

$$STF = \frac{k_{xcvc}k_{afe}k_Q T_d H_c}{1 + k_{xcvc}k_{afe}k_Q T_d H_c f_b} \qquad (2)$$

Assuming that the loop gain is large ($k_{xcvc}k_{afe}k_Q T_d H_c f_b \gg 1$) then the output will be equivalent to the applied input force.

B. Noise Transfer Functions

The noise transfer function in Equation (1) measures the noise contribution of each of the major noise contribution sources in the system. NTF_{En} measures the noise contribution of the AFE and is given by:

$$NTF_{E_n} = \frac{k_{afe}k_Q H_c}{1 + k_{xcvc}k_{afe}k_Q T_d H_c f_b} \qquad (3)$$

Equation (3) shows that the AFE noise contribution to the system is affected by the gain blocks k_{xcvc}, T_d and f_b. These gain blocks are signal translation block which converts a signal between different domains. E.g., T_d converts force to displacement, k_{xcvc} converts displacement to voltage and f_b converts voltage back to force, hence the overall signal gain is very small. Therefore, the noise contribution for the AFE block will directly appear at the output without much noise shaping from the ΔΣ operation.

NTF_{Qn} the noise transfer function for the quantizer is given by:

$$NTF_{E_n} = \frac{1}{1 + k_{xcvc}k_{afe}k_Q T_d H_c f_b} \qquad (4)$$

The quantizer used in our closed-loop operation is a one-bit quantizer and the quantization noise is one of the dominating noise sources in the system. From (4), the gain

blocks k_{afe}, k_Q and H_c provide the gain for NTF_{En}. k_{afe} is a scalar gain for in-band signal and AFE noise but it helps to improve the SNR with respect to the quantization noise Q_n. k_Q is a nonlinear gain term that has an inverse relationship to the magnitude of the signal at the input of the quantizer. H_c is transfer function for the electronic filter. Among the three gain blocks, H_c is the most crucial block for the reduction of the quantization noise in the system. It provides high gain for in-band signal but rejects out-of-band noise, hence it provides the noise-shaping function in the closed-loop operation with significant improvement to in-band SNR. The noise-shaping capability can be visualized from (4). H_c being the dominant gain term in the denominator, has integrator characteristic which provides large noise reduction and low-pass filtering for in-band noise. The noise corners are determined by the poles and zeros in the system. The poles and zeros introduced by the sensor is fixed by fabrication and needs to be compensated by the remaining poles and zeros from the electronic filter in order to maintain stability for the closed-loop operation.

III. PROPOSED ARCHITECTURE

Fig. 2 shows the proposed system architecture for a high-order closed-loop ΔΣ MEMS accelerometer. The proposed architecture contains an analog front-end (AFE) block to perform capacitance-to-voltage conversion, an N-bit analog-to-digital converter (ADC), a digital electronic filter block to perform ΔΣ modulation and phase compensation, and a feedback driver block to perform closed-loop MEMS control.
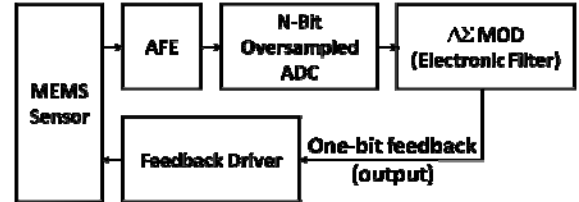

Fig. 2. The proposed system architecture for a high-order closed-loop ΔΣ MEMS Accelerometer.

From Fig. 2, the capacitive MEMS sensor is displaced from its nominal position when it experiences an external acceleration. This results in a corresponding capacitance change in the sensor which is converted and amplified into a voltage signal via the AFE block. The amplified analog signal is oversampled and converted into digital signal by the ADC block, and then passed to the digital electronic filter block for further signal processing. After the digital ΔΣ modulation and phase compensation, a 1-bit bit-stream is generated and fedback to the sensor through the feedback driver block. The feedback control signal restores the MEMS sensor back to its nominal position, ensuring high linearity measurement.

The electronic filter with a high gain makes dominant contribution to achieve wide dynamic range by increasing the order for the close-loop ΔΣ modulation system. However, it increases susceptibility to stability issues as additional poles and zeros are introduced into the loop. In this proposed architecture, the N-bit oversampling ADC conversion

enables digital implementation of the electronic filter to provide flexibility and configurability to deal with the close-loop stability issues with finer-tuning of the gain coefficients.
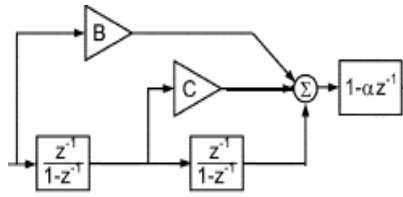

Fig. 3. A second-order electronic filter for feedforward high-order ΔΣ architecture

Fig. 3 shows the architecture of a second-order electronics filter for fourth-order ΔΣ MEMS accelerometer. The filter performs two-order ΔΣ modulation and phase compensation. The two-order ΔΣ modulation provides high gain only in the signal band and suppresses the out-of-band noise. Thus, the noise-shaping is achieved in the closed-loop operation to improve the in-band SNR significantly. On the other hand, the phase compensation is provided by the coefficient B, C and α. Coefficient B and C create a pair of complex zeros, while α contributes an independent controlled real zero [5]. By finding optimum relative values of B, C and α, the relative position of the compensating zeroes will be positioned in the pole-zero map of the overall fourth-order loop filter, so that the stability can be achieved while still maintaining desired wide dynamic range and high linearity.

Our digital ΔΣ modulator implementation is presented in Fig. 4. Fig. 4 shows the fixed-point implementation of a second-order electronic filer with 12-bit data, which is oversampled at a rate of 1024. Derived from Fig. 3, the reconfigurable digital electronic filter consists of a second-order ΔΣ modulator and a differentiator filter, as shown in Fig. 4 (a) and Fig. 4 (b), respectively. Its primary function is to perform second-order ΔΣ modulation in digital domain. This ΔΣ modulation converts the oversampled 12-bit ADC data into a multi-bit modulated data, of which effective number of bit (ENOB) is 21 bits. The modulated data is then quantized into 1-bit PDM (Pulse Density Modulation) bit-stream by using the most significant bit, which is a time encoded measure of the acceleration experienced by the MEMS sensor. The PDM bit-stream is to be used by the feedback driver to control the MEMS sensor in a closed-loop manner. To ensure the close-loop stability, a digital differentiator with configurable coefficient α is implemented to do phase compensation together with ΔΣ modulation coefficients B and C, as shown in Fig. 4.

As shown in Fig. 4, the digital electronic filter consisting of a ΔΣ modulator and a differentiator is implemented by a fixed-point Matlab Simulink model. The design and implementation are verified with a system-level floating-point model for a fourth-order closed-loop ΔΣ MEMS accelerometer. The ΔΣ modulator coefficients B and C, and the differentiator coefficient α, are configurable fixed-point parameters. In this implementation, the B, C and α are represented by 2's complement integer numbers and fractional number, which are sfix(1, 8, 0), sfix(1, 5, 0), and

sfix(1, 8, 7), respectively. The respective data range is [-128, 127], [-16, 15], and [-1, 0.9921875]. All the data computations required by the electronic filter are implemented by fixed-point arithmetic operations such as addition, subtraction, and multiplication, which are less expensive and likely consume lower power than analogue implementation.
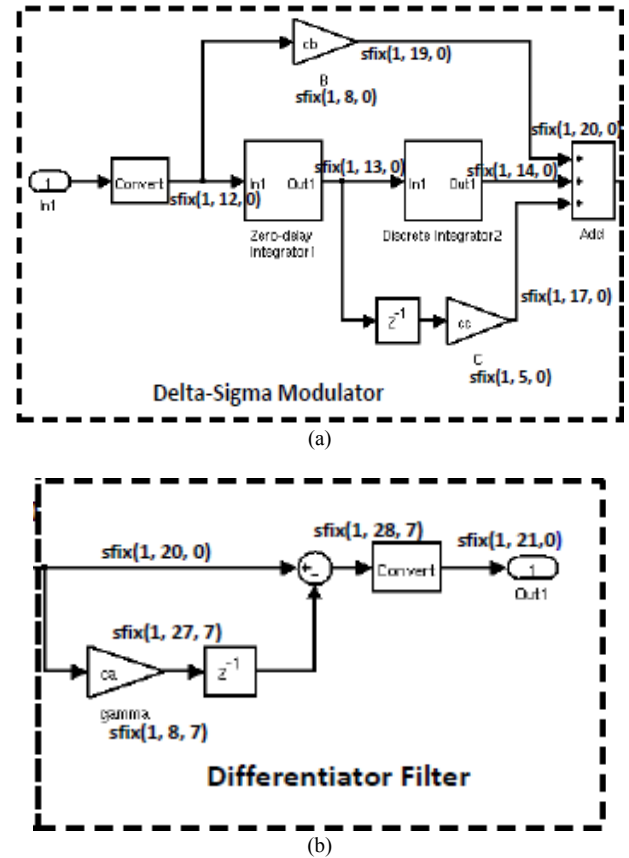

(a)

(b)

Fig. 4. Fixed-point implementation of the digital second-order electronic filter with 12-bit oversampled ADC data

IV. SIMULATION

Fig. 5 shows the transient simulation for the system with an input sinusoidal force applied to the closed-loop system. The feedback force (output) follows the input with a small transition delay. This transition delay comes from the implementation of the addition electronic filter H_c. This transition delay is an additional delay in the loop and care has to be taken during practical implementation to minimize loop delay as it affects the loop stability by reducing phase margin for the closed-loop operation.

Fig. 6 shows the simulation results of the *NTFs* for the electrical noise contribution from the AFE and the quantization noise from the one-bit quantizer. NTF_{En} shows that at low frequency (< 1kHz) the NTF_{En} has a gain of -20dB and this is the small noise gain coming from our MEMS sensor which shapes the low frequency noise contribution by a factor of 10 with the noise corner at approximately 1kHz.

The noise gain for NTF_{Qn} which determines the noise contribution from the one-bit quantization is significantly larger hence contributing to a large noise reduction to in-band quantization noise. From the simulation result, NTF_{Qn} at frequency below 1 Hz, the quantization noise reduction is
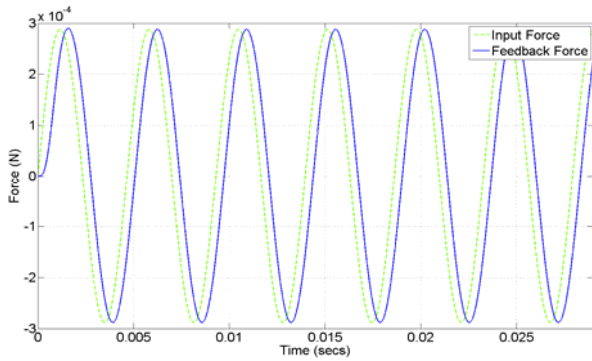
more than 180dB.

Fig. 5. Transient simulation for the closed-loop operation showing the feedback force with sinusoidal input force.
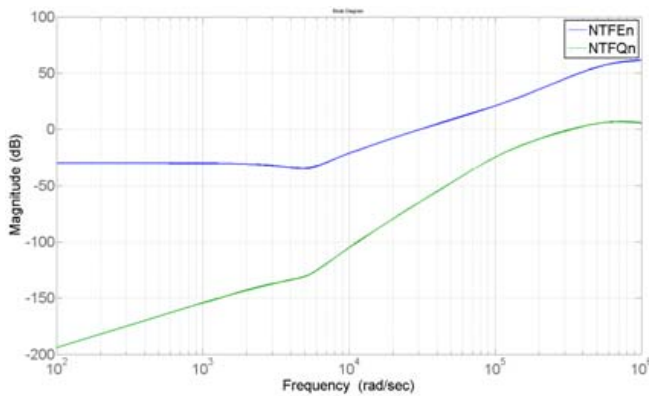

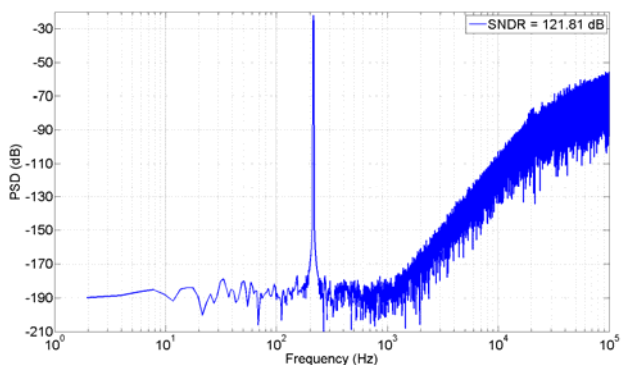Fig. 6. NTFs for the AFE noise and the quantization noise.

Fig. 7. Output power spectrum density for the closed-loop ΔΣ operation.

The large noise shaping characteristic comes from the two ideal integrators implemented in the electronic filter. These ideal integrators have infinite gain at low frequency hence causing the large gain reduction. In practice, these integrators will have limited gain and hence smaller noise reduction.

Fig. 7 shows the simulation result for the output power spectrum of the closed-loop system. With a full-scaled input, the system is able to achieve an SNDR larger than 120dB and an ENOB of 19.9bits.

V. EXPERIMENTAL RESULTS

A. First Order MEMS Model

For evaluation purposes, we built an evaluation board and MEMS mimic circuit to evaluate the performance of our closed-loop system. The evaluation board is built using a customized ASIC design consisting of only the AFE and feedback pulse drivers; discrete components consisting or an oversampled 12-bit coarse ADC and an FPGA. For the MEMS mimic circuit, we had a first order R-C filter and a second order L-C filter network. The R-C filter allows us to lower the loop order and hence establish the stability criteria of our closed-loop without the second order effects of the actual MEMS sensor. The L-C filter design resembles the MEMS sensor electrically with similar filter characteristics such as phase, resonant frequency and Q factor. The FPGA design realized the 12-bit input electronic filter of digital ΔΣ modulation and phase compensation, as shown in Fig. 4.
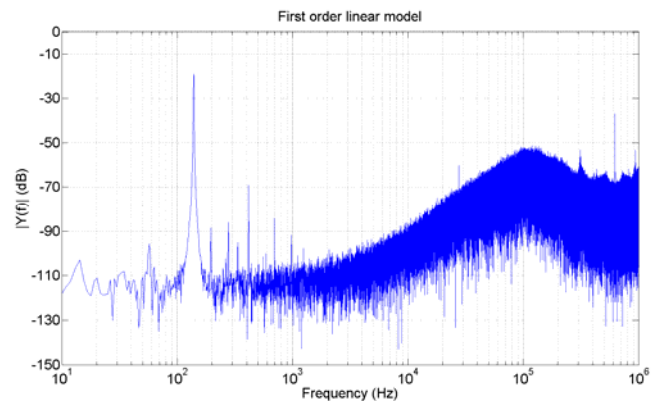

Fig. 8. Output power spectrum density from the measurement with a first order R-C MEMS mimic.

Fig. 8 shows the output power spectrum density measured from the R-C first order MEMS mimic. The noise shaping characteristics are similar to simulation with the noise corner at about 1 kHz. This noise corner is set by the R-C network. The SNR achieved is more than 90 dB but harmonic distortion is clearly visible and this can significantly degrade the ENOB reading.
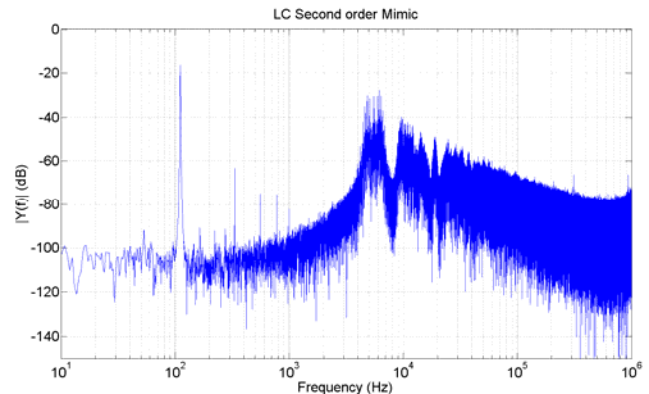

Fig. 9. Output power spectrum density with a second order L-C MEMS mimic circuit.

Fig. 9 shows the result taken from the L-C second order MEMS mimic. Similar to the result from the R-C MEMS mimic, the noise shaping characteristic is also present with the noise corner set by the resonant frequency of the L-C network. For the L-C MEMS mimic, an SNR of less than 90dB was measured. The decrease in the SNR is caused by the increase in the in-band noise floor as well as the noise corner. The system for the L-C MEMS mimic has a higher loop dynamics than the R-C MEMS mimic. However, the additional loop order for the L-C MEMS does not provide a noise gain and hence can reduce the effectiveness of

electronic filters if the poles and zeros are not optimally placed.

VI. CONCLUSION

We have presented a high order closed-loop capacitive MEMS accelerometer design. The closed-loop operation is based on the $\Delta\Sigma$ loop design consisting of the MEMS sensor as part of the loop dynamics and additional electronic filters to reduce the noise contribution from the one-bit feedback quantizer. Our electronic filters are implemented digitally and that gives us better flexibility in choosing the filter characteristics to optimize the system performance both in stability of the loop as well as the reduction of in-band noise due to quantization. We showed that in our system are able to achieve > 120 dB SNDR performance in simulation and > 90 dB SNR for an evaluation version using MEMS mimicking circuit. Our next step is to integrate our system fully in ASIC with actual MEMS sensor.

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