Dual Negative Regulated Charge Pump

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***Abstract*—This paper presents a Dual Negative Regulated Charge Pumps which is insensitive to process and temperature variations. The Dual Negative Charge Pump makes use of two PMOS transistors to switch on either one of the two negative outputs. The negative charge pump was realized with good line regulation, low ripple voltage and small IC area. Measurement and simulation results show that the Dual Negative Charge Pump meets all the design specifications.**

***Index Terms*—Negative charge pump, regulated, fixed frequency, constant switching frequency.**

I. Introduction

In a RF receiver, a Pseudomorphic High-Electron Mobility Transistors (PHEMTs) [1] is usually used in the first stage to provide low noise figures and high gain, in particular at millimeter-wave frequencies. For most of the receivers, the IC and PCB are usually small in size and has to operate under harsh environment. Hence, the LNA in the receiver has to be designed with stringent design requirements which include simple construction, small form factor, low noise, wide band, high linearity, unconditionally stable, high reverse isolations and high frequency coverage.

To ensure good overall performance, it is important to ensure that the operation of the PHEMT is stable at all frequencies. Since the PHEMT is the first stage of the LNA, it is important to ensure that the PHEMT is biased at the correct voltage and the bias voltage is insensitivity to input voltage and temperature variation.

Fig 1 depicts the I_D-vs-V_{GS} characteristics of a PHEMT. From the graph, it can be observed that any change in the gate-to-source voltage will affect the drain current of the PHEMT. The I_D variation is approximately 0.1mA/mV. Hence, it is necessary to design a negative bias network for the PHEMT which is less sensitive to supply voltage and temperature variations.

To overcome the challenges, we propose a regulated Negative Charge Pump (NCP) which is less sensitive to supply voltage and temperature variations. The motivation of this invention is to design a negative charge pump with the following characteristics: small IC area, good line regulation, insensitive to temperature variation, low ripple, fixed switching frequency. To ensure that the switching frequency of the charge pump introduces minimal noise and interference to the RF chain, the switching frequency is derived from the clock of the PLL so that it is synchronized with the clock frequency of the PLL. Hence, the negative charge pump will operate on the basis of fix switching as opposed to variable switching frequency which were reported in some papers [2]-[3].

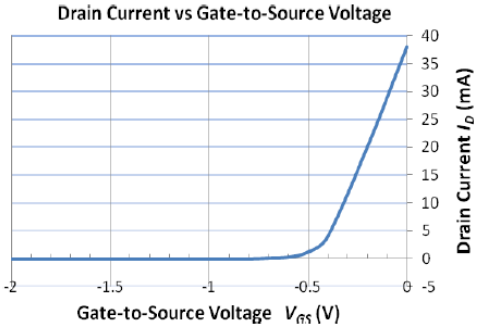

Fig. 1. *ID*-vs-*VGS* characteristics of a PHEMT.

II. Integrated Negative Charge Pump

A. Single Stage Negative Charge Pump

The schematic of the Negative Charge Pump is depicted in Fig 2. It consists of an error amplifier, a charge pump Capacitor C_p, two transistors for charging the capacitor (P_1 and N_1), two diode connected transistors (N_2 and N_3), a non-overlapping clock generator, an OR gate and a 1.2V-to-3.3V level-shifter.

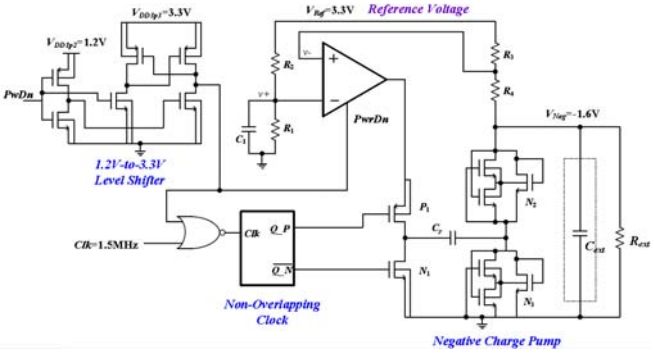

Fig. 2. Schematic of the -1.6V Negative Charge Pump.

The operating principles of the Negative Charge Pump are as follows. The reference voltage of the Negative Charge Pump at the negative input of the error amp is set by the resistor divider, R_1 and R_2, which is connected to a 3.3V positive input voltage supply. The positive input of the error amplifier is connected to another set of resistor divider, R_3 and R_4, to monitor the voltage level at the negative output. Since the output voltage is negative while the input to the amplifier is positive, the reference of the resistor divider is

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tied to the 3.3V supply voltage. Due to temperature variation, the 3.3V supply voltage will drift when the temperature varies from -40˚C to 85˚C. To mitigate the effect of supply voltage variation, the reference voltage (R_1 and R_2) and the feedback resistor network (R_3 and R_4) are tied to the same 3.3V supply [5]. By means of negative feedback, the error amplifier will generate the required voltage to charge up the capacitor, C_P, via the pMOS transistor.

The pMOS and nMOS transistors, P_1 and N_1, are controlled by a non-overlapping clock generator to ensure that the two transistors are not turned on at the same time. During the charging phase, transistor P_1 is turned on and capacitor C_p is charge up via P_1 and the diode connected transistor, N_1. During the discharging phase, transistor P_1 will turn off and N_1 will be turned on. Since, N_1 connects one terminal of C_p to ground, the other terminal of C_p will be negative. This negative terminal will charge the output to a pre-defined negative voltage via the other diode connected transistor, N_2. As the negative charge pump is only used for biasing the gate of the PHEMT, the load resistor is considerably large (~ 400kΩ) to reduce the bias current. Since the load resistor is large and has a fixed value, it can be used together with the external load capacitor to set the dominant pole of the feedback loop. For example, if R_{ext}= 400kΩ and C_{ext}=1nF, the dominant pole of the feedback loop will be 398Hz. As the second pole of the op-amp is a few decades apart, the feedback loop will be inherently stable. This will save a substantial amount of IC area that is required for the compensation capacitor to create the dominant pole.

The negative charge pump can be disabled by a power down control signal. As the power down signal comes from a 1.2V logic while the NOR gate of the negative charge pump is a 3.3V logic, a level-shifter is required to step-up the voltage of the power down control signal from 1.2V to 3.3V.

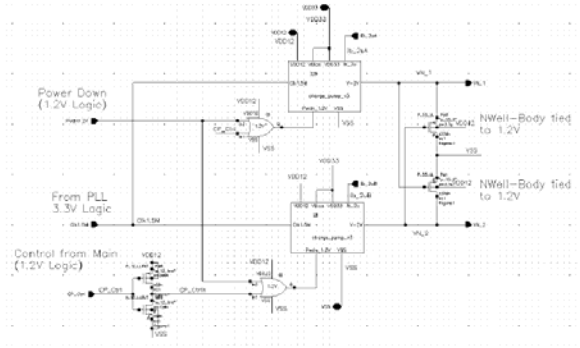


Fig. 3. Schematic of the dual negative charge pump.

B. Dual Negative Charge Pump

The RF chains consist of two bands, namely the low band and the high band. Hence, two PHEMTs are used at the front-end of the RF chain, to provide option for the selection of the low band or the high band. To cater for this selection, a Dual Negative Charge Pump comprising two identical Negative Charge Pumps as depicted in Fig 5 is used to bias each of the PHEMTs. To improve the efficiency and reliability of the circuit, one of the Negative Charge Pump will be disabled via the power down control pin. The control logic for the power down includes an inverter and two OR gates as shown in Fig. 3. The two PMOS transistors at the output of the Negative Charge Pump are used to set the output of the charge pump to 0V when the Negative Charge Pump is disabled. One of the difficulties in this project is the generation of negative voltage to control the gate of the PMOS switches. In this design, the -1.6V output of the active NCP will turn on the PMOS transistor of the other NCP and short its output to 0V. Hence, the arrangement will automatically set the output of the inactive NCP to 0V.

III. Simulation and Measurement Results

The performance of the Dual Negative Charge Pump was simulated and measured for the test chip and the full chip embodying all the RF circuit blocks.

The IC Layout of the Dual Negative Charge Pump is depicted in Fig. 4. The dimension of the IC is 160m by 215m without bond pads. The microphotograph of the Dual NCP is depicted in Fig. 5.

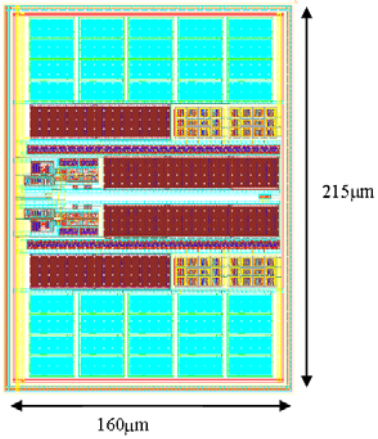


Fig. 4. IC Layout of the dual negative charge pump.

Fig. 6 depicted the measurement output voltage at the two outputs of the Dual Negative Charge Pump across the temperature range from -40˚C to 85˚C. From the figure, note that the variation of the output at -1.6V is about 10mV. The voltage variation of the other output stage (~3mV @ 8mV) is not important since it has been disabled.

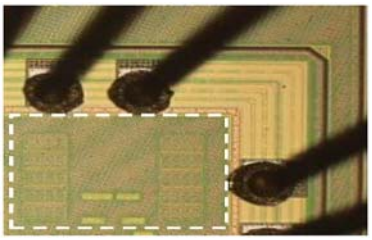
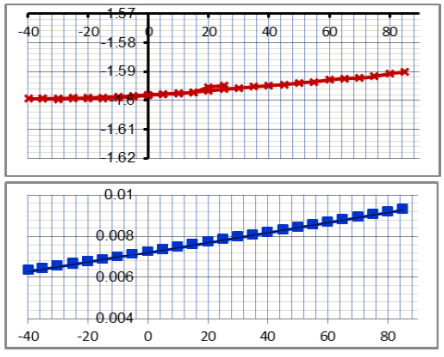


Fig. 5. Microphotograph of the Dual Negative Charge Pump.

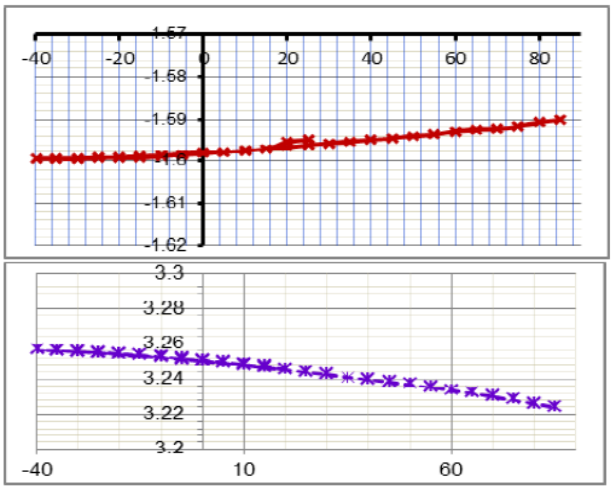


ΔV @ −1.6V= 10mV (Temp: 40˚C to 85˚C)

Fig. 6. Output voltages of the dual negative charge pump over the temperature range from -40˚C to 85˚C.

TABLE I: SIMULATION AND MEASUREMENT RESULTS.

Items	Sym.	Conditions	Typ.	Simulat-ion	Measure-ment	Unit
Input Voltage	V_{in}		3.3	3.3	3.3	V
Output Voltage1	$V_{out}1H$	ON (@ 25˚C)	-1.6	-1.6	-1.596	V
	$V_{out}2L$	OFF (@ 25˚C)	0	0.005	0.007	V
Output Voltage 2	$V_{out}2H$	ON (@ 25˚C)	-1.6	-1.6	-1.583	V
	$V_{out}2L$	OFF (@ 25˚C)	0	0.005	0.007	V
Ripple Voltage	V_{ripple}	R=400 kΩ, C=1μF	<25mV	0.001	0.01	V
Clk Freq	f_{sw}		1.5	1.5625	1.5	MHz



ΔV= 10mV (Temp: -40˚C to 85˚C)

Fig. 7. Output voltage of the negative charge pump and the 3.3V LDO over the temperature range from -40˚C to 85˚C.

Fig. 7 depicted the measured output voltage of the Negative Charge Pump and the 3.3V LDO over the temperature range from -40˚C to 85˚C. The variation of the 3.3V LDO is about 30mV, yielding a temperature coefficient of about 80V/C.

This shows that the design of the Negative Charge Pump which uses a resistor divider to set the reference has effectively reduce the variation of the -1.6V output voltage.

The transient response of the Negative Output voltage across three different corners is depicted in Fig 8. The variation of the output voltage for the three different corners is quite small, about 0.1mV. The ripple of output is about 0.7mV and it can be further reduced by using a bigger load capacitor at the output.

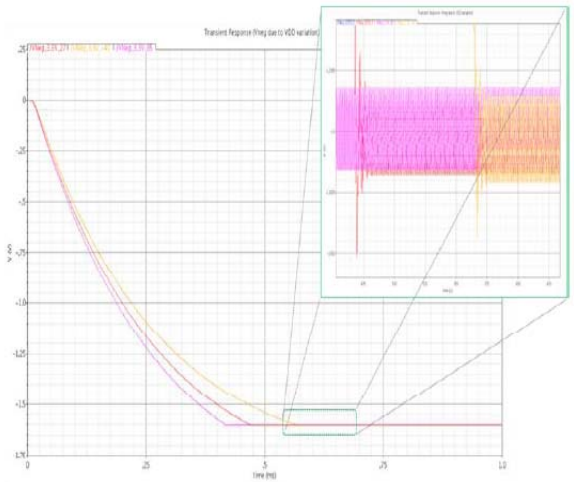
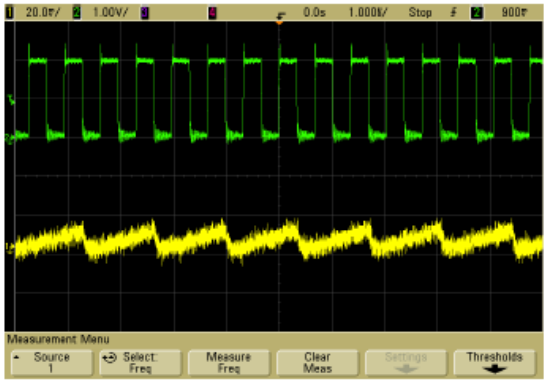


Fig. 8. Transient response of the negative output voltage at three difference corners: fast fast (-40˚C, Orange), typicaltypical (27˚C, Red), slowslow (85˚C, pink).

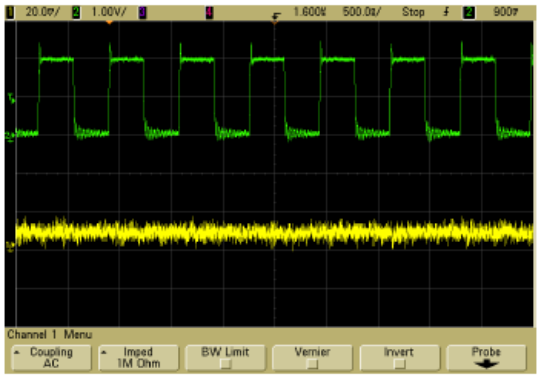
Fig. 9. Transient response of the two outputs due to switch control.

The transient simulation output waveforms of the two complementary outputs when they are enabled or disabled are depicted in Fig 9. The waveform of the first NCP is highlighted in purple whereas the waveform of the second NCP is highlighted in yellow.

Fig. 10 depicts the output voltage of the Negative Charge Pump using different load capacitor. From Fig 10, it can be seen that the ripple voltage can be effectively reduced by using a large load capacitor.



(a) R=400kΩ, C=1nF



(b) R=400kΩ, C=1μF

Fig. 10. Measured output voltage of the Negative charge pump.

The simulation and measurement results of the negative charge pump are tabulated in Table 1. From Table 1, the output voltage of the output 1 and 2 is -1.596V and -1.583V, respectively when negative charge is turned ON. The output voltage of output 1 and 2 is 0.007 when they are turned OFF, thereby showing that the proposed design meets the design specifications.

IV. Conclusion

We have proposed a regulated Negative Charge Pump based on constant switching frequency. Measurement on the output over the temperature range from 40˚C to 85˚C showed that the Negative Charge Pump is able to provide a regulated voltage of -1.6V with a temperature coefficient of 80μV/C. The variation of the output voltage at the extreme corners is 0.1mV. The ripple voltage at a switching frequency of 1.5MHz is about 20mV and 10mV for a load capacitor of C=1nF and C=1μF, respectively. This ripple can be reduced by increasing the load capacitor at the output without affecting the stability of the feedback loop.

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