Floating-Gate Operational Transconductance Amplifier

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***Abstract*—A configuration of operational transconductance amplifier (OTA) based on floating-gate MOSFETs for low-power, low-voltage, and low-frequency applications is presented in this paper. The main features of the proposed OTA are design simplicity and rail to rail input voltage at supply voltage of ±0.5 V. The proposed OTA has high output impedance, good stability, and reduced power consumption of 36 µW. PSpice simulation results using 0.18 µm CMOS technology are presented to prove the results achieved, and in the light of them, the major characteristics of the circuit are manifested.**

***Index Terms*—Floating-gate MOSFET, low voltage, low power, threshold voltage, OTA.**

I. Introduction

Circuit designers nowadays face great challenges since the users of technology increase more and more. The desire for portability of electronic equipment generated a need for low power systems in battery-operated products, so the need of circuits that dissipate low power is arising significantly because low power consumption is essential in these applications to have reasonable battery life and weight, thus the main interest is to minimize power consumption of the circuits. Anyhow, average power, P_{avg}, consumed by these circuits consists of the sum of two components, static and dynamic power [1]:

$$P_{avg} = P_{static} + P_{dynamic} = V_{DD} I_{leakage} + C V_{DD}^2 f \quad (1)$$

where V_{DD} is power supply voltage, $I_{leakage}$ is sub-threshold leakage current of MOSFET transistor, C represents the total capacitance of a system, and f denotes the frequency at which a circuit operates, and since $I_{leakage}$ is exponentially dependent upon the threshold voltage of the transistor, V_T, the obvious way to achieve low power dissipation would be to operate them at low supply voltages, i.e. to reduce power supply voltage, V_{DD}.

Thus, as of yet, no effort has been undertaken to achieve this aim, many design techniques for low-voltage low-power analog circuits are used by designers, for instance, the level shifter techniques [1], [2], bulk-driven transistors [1]-[3], MOSFETs operating in the sub-threshold (weak inversion, cut-off) region [1], [2], [6], self-cascade structures [2], [3], and floating-gate approach [1]-[5], [7]. This paper is aiming to concentrate on the last item, floating-gate MOSFETs.

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II. Floating-Gate Mosfets

Floating-gate MOSFET transistors are widely used in digital world as EPROMs (Erasable Programmable Read Only Memories) and EEPROMSs (Electrically Erasable Programmable Read Only Memories), that was the case for decades, but the trend these days is to use them as circuit elements, as it will be shown in this paper.

The layout, circuit symbol, and equivalent circuit of a multi-input floating-gate MOSFET are shown in Fig. 1. Until recently, FG transistors had only been used in digital electronics EEPROM devices and despite the important role FG-MOSFET devices could play in analog circuits, designers have been reluctant to work with them. The main reason for this is the uncertain amount of charge (Q_{FG}) that might stay trapped at the FG during the fabrication process causing variations of the threshold voltage. Q_{FG} has different implications on different circuits; however, the design will often not work unless the charge is removed, this charge can stay there for several years with the variation of less than 2% in room temperature [2]-[4], [7]. Reported solutions to remove Q_{FG} include cleaning with ultraviolet (UV) light shining [2]-[4], [7], hotelectron injection [2], [3], [7], Fowler-Nordheim (FN) tunneling [3], [4], [7], and forcing an initial condition with a switch [7].

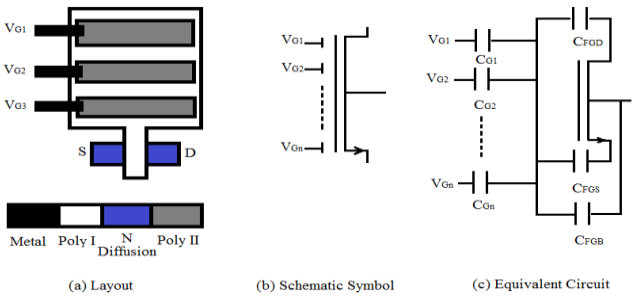

Fig. 1. Multi-input floating-gate MOSFET

The floating gate voltage is given by [1]:

$$V_{FG} = \frac{Q_{FG} + C_{FGD} V_D + C_{FGS} V_S + C_{FGB} V_B + \sum_{i=1}^{n} C_{Gi} V_{Gi}}{C_{TOTAL}} \quad (2)$$

where V_{Gi} is voltage of the ith control gate and C_{TOTAL} is the total capacitance which is given by

$$C_{TOTAL} = C_{FGD} + C_{FGS} + C_{FGB} + \sum_{i=1}^{n} C_{Gi} \quad (3)$$

where C_{FGD}, C_{FGS}, and C_{FGB} denote the capacitances from gate to drain, source, and bulk respectively. V_D, V_S, V_B are drain, source, and bulk voltages. C_{Gi} is the capacitance coupling between each input gate and the floating gate, and

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V_{Gi} is the voltage applied at input gates.

For a two-input FG-MOSFET, a higher DC voltage V_b is applied at one gate (bias gate) through C_{G1} and the signal is applied at the second gate (signal gate) through C_{G2} (see Fig. 2(a)). Assuming zero initial charge and neglecting parasitic capacitances as compared to C_{G1} and C_{G2}, the gate voltage is:

$$V_{FG} \approx k_1 V_{in} + k_2 V_{bias}, \quad (4)$$

where $k_1 = \frac{C_{G1}}{C_{TOTAL}}$ and $k_2 = \frac{C_{G2}}{C_{TOTAL}}$.

The equivalent threshold voltage for the MOSFET adjusts itself to a new value $V_{T,eq}$:

$$V_{T,eq} = \frac{V_T - V_b k_1}{k_2} \quad (5)$$

It is obvious that $V_{T,eq}$ will be less than V_T if V_b, k_1, and k_2 are properly selected. Thus it is possible to get a MOSFET where V_T is lower than the normal V_T. The effective transconductance is given by:

$$g_{m,eff} = k_2 g_{m,FG} \quad (6)$$

where $g_{m,FG}$ is the transconductance seen from the floating gate. Note that $g_{m,eff}$ is less than $g_{m,FG}$ by a factor of k_2.

When g_o is the output conductance of a MOSFET, the effective output conductance $g_{o,eff}$ of the floating-gate MOSFET is:

$$g_{o,eff} = g_o + g_{m,FG} \frac{C_{FGD}}{C_{TOTAL}} \quad (7)$$

Because there is DC and AC feedback from drain to floating gate through C_{FGD}, the output impedance is less than that of a MOSFET working in the same biasing condition.

Depending on the applied bias voltage V_{bias} on the floating terminal, the threshold voltage level of the MOSFET is shifted.

Fig. 3 shows the drain currents versus gate–source voltages of the floating-gate and conventional (gate-driven) common-source amplifier shown in Fig. 2 simulated for V_{bias} = 1 V.

We notice from Fig. 3 that FG-MOSFET begins to conduct current when the gate-driven MOSFET is still closed or off.

For example: for V_{GS} = 176.8 mV, I_d equals 100 μA for the FG-MOSFET whereas it equals 24 nA for the conventional one.

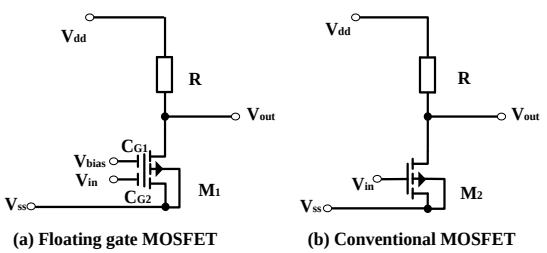

Fig. 2. Common-source amplifier

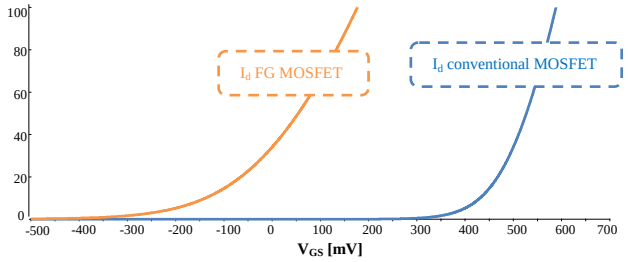

Fig. 3. Id [μA] vs. VGS

For more illustration, assuming the features of FG MOSFET in numerical values are: FG-MOSFET in Fig. 2 has W/L = 50 μ/2 μ, $C_{bias} = C_{in}$ = 0.2 pF, C_{FGD} = 43.6 fF, C_{FGS} = 4.36 fF, C_{FGB} = 20 aF, V_T = 0.366 V, $g_{m,FG}$ = 540 μS, and g_o = 2.95 μS.

Substituting these values in the previous appropriate equations yields the following:

$C_{TOTAL} \approx C_{bias} + C_{in}$ = 0.4 pF and $k_1 = k_2$ = 0.2 pF/0.4 pF = 0.5.

The equivalent threshold voltage is: $V_{T,eq}$ = 0 V for V_{bias} = 0.732 V.

As we have just seen, we can remove the threshold voltage. More than that, we can make it negative for some other value of bias voltage as folloiwng:

$V_{T,eq}$ = ±0.068 V for V_{bias} = 0.8 V. This property makes the FG technique one of the most attractive methods for low voltage design.

The effective transconductance is: $g_{m,eff} = 0.5 g_{m,FG}$ = 270 μS.

The effective output conductance is: $g_{o,eff}$ = 61.81 μS.

The equations and numerical values show the advantages and the disadvantages of the FG-MOSFET compared with the conventional gate-driven MOSFET.

III. Operational Transconductance Amplifier Based on FG-Mosfets

Operational Transconductance Amplifier or OTA is a key functional block used in many analog and mixed-mode circuits. In point of fact, it is usually more desirable than any ordinary amplifier because of its high output impedance as we will see later. Anyhow let us describe the proposed configuration and its function in some detail. The circuit presented here is a two-stage transconductance amplifier. The scheme uses p-channel floating-gate transistors at the input, M_1 and M_2, each with two gates. Of course, it is possible to use a complementary scheme with n-channel input transistors. As specified by the name, the circuit is the cascade of two stages: The first is a differential amplifier which consists of input devices M_1, M_2 and the current mirror M_3, M_4 which is acting as an active load, the second stage is a conventional inverter with M_5 as a driver and M_6 as an active load. See Fig. 4.

The current of M_1 is mirrored by M_3, M_4 and subtracted from the current comes from the drain of M_2, then the signal contributions of the two currents multiplied by the output resistance of the first stage give the single-ended first stage output voltage. This resulting signal constitutes the input of the second gain stage.

Transconductance of the OTA is 1.97 mA/V. It is important to notice here that all transistors must still be working in the saturation area all the time. Compensation capacitor C_C takes care of compensation requirements since it connects gain stage's output of the OTA with its input. By the means of C_C we shift down the dominant (first) pole's frequency from 100 kHz to 3 kHz which consequently enhances the stability of the circuit since it affects phase margin (*PM*) value as explained in the following equation [7]:

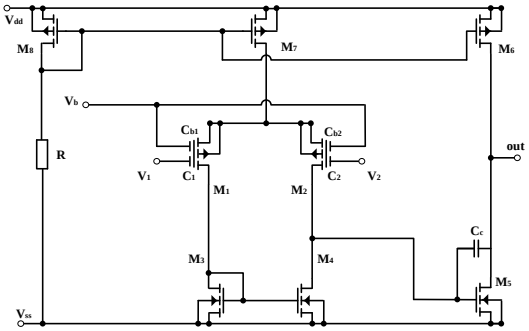

Fig. 4. The circuit of two-stage OTA using FG-MOSFETs

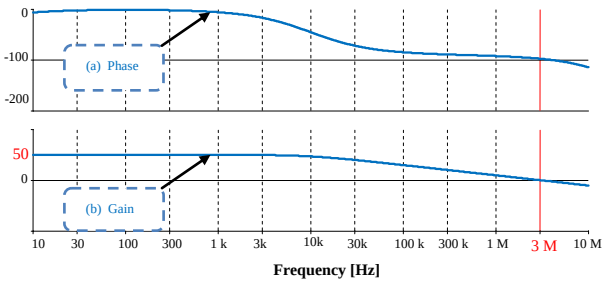

Fig. 5. Frequency response of OTA: (a) Phase [◦], (b) Gain [dB]

$$PM = \pm 180 - a\tan\frac{GBW}{|W_{P1}|} - a\tan\frac{GBW}{|W_{P2}|} \qquad (8)$$

where w_{p1} and w_{p2} are the angular frequencies of the first and second poles, respectively. Indeed, stability is paid for by a reduction in the gain bandwidth because lowering dominant pole's frequency would reduce it, but we had to take a decision here for some trade-off between the conflicting requirements of gain bandwidth and stability.

The performance of the circuit is summarized in Table I. The values of the input capacitances for the circuit, compensation capacitance, bias voltages, and resistance used are collected in Table II.

The MOSFETs used in simulation are BSIM3 model version 3 (level 7). The estimated parasitic capacitances via simulations are: C_{FGS} and C_{FGD} are 6.92 fF each and C_{FGB} is 0.2 aF. Table III illustrates the dimensions of transistor components as well as their biasing currents.

The numbers speak for themselves, in the case of this specific design the following specifications are acquired: a power consumption smaller than 40 µW, gain-bandwidth product larger than 3 MHz for a load of 1 pF, phase margin greater than 60◦, gain slightly over 50 dB, and a maximised input range. The minimum voltage supply is in this case determined by the common mode input range that requires a minimum value of 1V.

Voltage gain A_V and unity gain frequency *GBW* are shown in Fig. 5(a) and (b), and reffered to by red numbers.

A point that is worthwhile underlining is that in practice, and since we should use capacitors in input stage, this OTA has no DC gain because it simply does not have DC input signal.

The most important factor which necessary very much indeed to take into account is the matter of stability, which in turn is very well achieved in the circuit, one can observe from Fig. 5 that the phase at the unity gain frequency is about 100◦, so the phase margin is about 80◦which is more than the minimum allowable limit (60◦) [6], and that puts us in the safe side and makes us more confident with this simple configuration.

The input range has been determined with the OTA connected as a buffer, and a 10 kHz sinusoidal input signal, allowing a maximum total harmonic distortion (THD) at the output of 0.93%. Both signals are depicted in Fig. 6 wherein the solid blue curve (a) denotes the input signal and the long dash orange curve (b) refers to the output one. We notice from Fig. 6 that the configuration has rail to rail operation for 1V input signal, the negligible offset voltage has the very small value of 179 µV, this unavoidable offset can be explained by offset contributions from transistor components, especially from differential pair and current mirror.

TABLE I: SUMMERY OF THE PERFORMANCE FOR THE OTA

Voltage supply	1 V
Voltage gain	51 dB
CMRR	63 dB
Offset voltage	179 µV
GBW	3.15 MHz
Phase margin	82◦
Power consumption	36 µW
Slew rate	2.3 MV/s
Settling time	800 ns
Input range	0.8 V_{pp} = 0.78 V_{DD}

TABLE II: MEASUREMENT CONDITIONS OF THE CIRCUIT

Parameter	Value
C_{b1}, C_{b2}	0.3 pF
C_1, C_2	0.1 pF
C_c	1 pF
V_b	– 0.3 V
R	50 kΩ

TABLE III: OTA TRANSISTORS DIMENSION

Device	Type	L/W [µm]	I_d [µA]
M_1, M_2	PMOS	0.2/10	4.5
M_3, M_4	NMOS	0.8/10	4.5
M_5	NMOS	0.8/10	18.6
M_6	PMOS	0.6/40	18.6
M_7	PMOS	0.6/20	9
M_8	PMOS	0.6/20	9.5

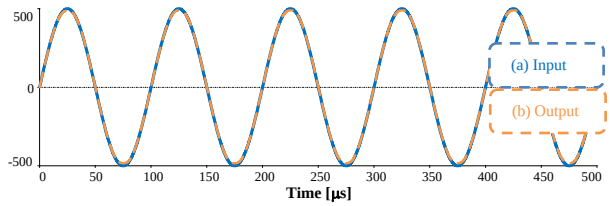

Fig. 6. Input and output signals [mV] vs. time

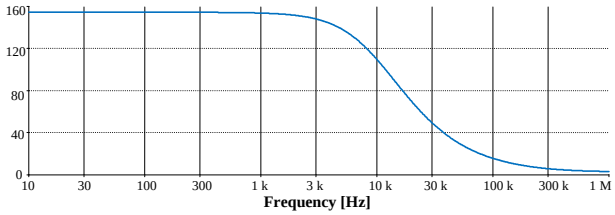

Fig. 7. Zout [kΩ] vs. frequency

With a value close to 160 kΩ, the high output impedance is also existed, compared with just a few tens of ohms which its normal operation amplifier match can perform, and that makes OTA more desirebale than any ordinary amplifier as it was mentioned earlier. Fig. 7 shows us the curve of Z_{out}, please observe the value of impedance at low frequency, which is R_{out}.

Finally, it is necessary to be mentioned, that we face a practical problem when we design an OTA based on FG-MOSFETs, it consists in that the amount of layout area consumed by the floating gate MOSFET is a concern since C_1 and C_2 are required to be at least ten times larger than the floating gate oxide capacitance in order for the device to operate properly [1].

IV. Conclusions

The advantages and disadvantages of two-input floating-gate MOSFET in comparison with conventional MOSFET are highlighted. In spite of the fact that floating-gate MOSFET needs just few hundred millivolts to be in saturation, it loses a lot of its input transconductance. Moreover, there is remarkable reduction in its output impedance.

A simple OTA using floating-gate input MOSFETs is simulated using PSPICE program, this OTA is so called low-power low-voltage OTA because it operates under 1 V voltage supply and dissipates less than 40 µW. The gain of the proposed OTA is about 50 dB, which not high enough for many applications. However, it can be considered as acceptable. The gain in bandwidth is relatively low (3.15 MHz) but enough for low-frequency applications such as in biomedical field, the proposed OTA offers rail-to-rail voltage swing at ±0.5 V, the output impedance is high, and the circuit is stable.

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