Design of a High Performance 5.0 GHz Low Phase Noise 0.35 μm CMOS Voltage Controlled Oscillator

Mohammed A. Aqeeli and Zhirun Hu

***Abstract*—This paper describes how a novel low phase noise Figure of Merit (FOM), LC-tank voltage-controlled oscillator (VCO) is presented. The work presents a fully integrated 5.0 GHz VCO designed in a 0.35 μm CMOS process. The proposed VCO features a worst-case phase noise of -133.07 dBc/Hz and -136.31 dBc/Hz at 600 kHz and 1 MHz frequency offset. An optimization technique is used to design the excellent FOM. The FOM is -206. 20 dBc/Hz. It features a supply of 2.4 V, a core of only 1.0 mA.**

***Index Terms*—Design method, figure of merit, low phase noise, tuning range.**

I. Introduction

VCOs have become one of the most important components of today's communication systems. They are among the key building blocks of RF systems. They are used for carrier frequency synthesis to up-convert and down-convert signals. Their output frequency is stabilized or controlled with a Resonator. The increasing demand for wireless and multimedia applications is motivation for designing the CMOS integrated wireless systems to support and achieve many communication standards such as WLAN and GSM.

Further, the exponential growth in this market has brought an increasing demand for high-performance, low-cost radio-frequency technologies. In view of the continuous development and wide improvements in CMOS VCOs, it is now generally recognized that they still remain the most critical part of RF transceivers. Tuning range, tuning gain and phase noise are the important characteristics of a VCO. In general, low phase noise is preferred in the VCO. The phase noise of the VCO is one of the most important parameters for the quality and performance of information transfer, in turn affecting the reliability purposes in data communication. Consequently, achieving low phase noise and low power consumption specifications, VCOs are a major design challenge and thus have received a lot of attention in recent years. Many have tried to improve the phase noise performance of LC-VCO [1]-[4]. To achieve the low-phase-
noise specifications, the integrated LC-VCO seems to be the best choice. The design depends specifically on the integration of a high-quality LC tank.

This paper is organized as follows: first we present the circuit design considerations used to minimize the phase noise, then we show the realization and measurement results. Finally, we conclude the paper with a performance summary and comparison with the state-of-the art designs.

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M. A. Aqeeli and H. Zhirun are with the The University of Manchester, Manchester, UK (e-mail: mohammed.aqeeli-3@postgrad.manchester.ac.uk, Z.Hu@manchester.ac.uk).

II. VCO Design and Implementation

Fig. 1 shows the standard LC-VCO design. The implemented VCO uses a complementary cross-coupled topology. The performance was implemented in a standard 0.35 μm CMOS process.

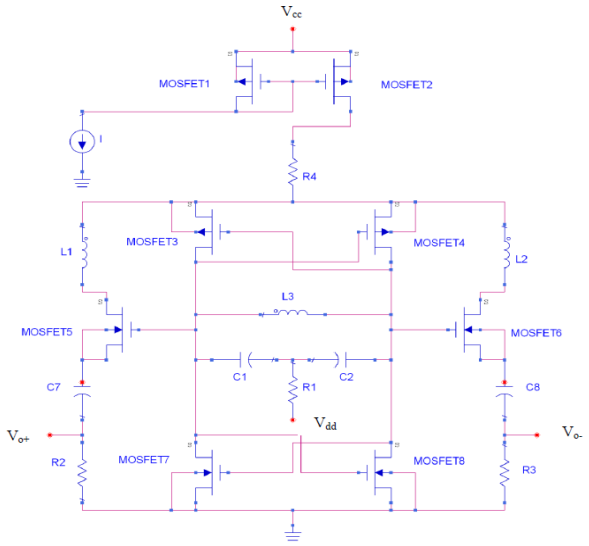

Fig. 1. Complementary cross-coupled VCO

The circuit topology of this VCO was selected for two reasons: first, the suitability for low-power; and second, the loss of the LC tank will be compensated by the cross-coupled NMOS and PMOS differential pairs which provide a negative resistance and generate symmetric signals [5]. Inductance and capacitance of the LC tank were determined and the targeted center frequency was chosen to be 5.0 GHz.

The utility of MOSFETs as controllable resistors and, for this reason, switches plays a crucial role in many analogue circuits. The current is given by:

$$I_D = \mu_n C_{ox} \frac{W}{L} [\,(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2] \qquad (1)$$

This equation indicates that the current capability of the device increases with V_{GS} and the peak current occurs at $V_{DS} = V_{GS} - V_{TH}$ which is called the overdrive voltage [6].

The challenge of this design was to reduce the phase noise of the previous work accomplished. Therefore, some techniques and several steps were taken into consideration

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in order to achieve the best phase noise. Firstly, the tail transistors of the current mirror design were implemented using PMOS (MOSFET1-MOSFET2) components which offer a high precision current source, and the noise is less than the NMOS mirror current circuit. Secondly, transistor sizing was used to control the VCO current. In addition, the areas of the cross-coupled pair were kept slightly high to reduce 1/*f* noise. Thirdly, it is obvious that Q_L of the LC tank will greatly affect the phase noise performance. The inductor was near optimum for the oscillator design at around 0.2nH, as will be seen later. Relatively small L and high Q inductor values are the key to a good, low-power, low-noise oscillator. Finally, keeping the gm of the NMOS and PMOS at the same value helped to reduce the up-conversion of the phase noise. The VCO outputs are buffered using buffer stages NMOS (MOSFET5-MOSFET6) to isolate the LC tank. The required transconductance for VCO startup can be reduced, leading to the minimized dc power for sustaining VCO oscillation.

The total capacitors of this design are approximately 5.0pF to tune the oscillator. Most of the parameters are process dependent, and there are a few circuit parameters we can control, namely, the channel length and channel width of the transistors, and the LC tank's quality factor. The physical dimensions *W/L* (the aspect ratio) of the MOSFETs are maintained at 6.0 μm/0.35 μm for optimum phase noise. The measured results demonstrate that the topology in this research is useful for achieving a lower phase noise.

Since a MOSFET operating in saturation produces a current in response to its gate source overdrive voltage, a figure of merit (FOM) which indicates how well a device converts a voltage to a current can be defined as the change in the drain current divided by the change in the gate to source voltage [6]. This fraction is called transconductance and is denoted by g_m ,, a quantity expressed as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}} = \mu_n C_{ox} \frac{W}{L} [\,(V_{GS} - V_{TH}) \qquad (2)$$

g_m represents the sensitivity of the device for a high transconductance; a small change in results in a large change in. The double cross-connect NMOS (MOSFET7-MOSFET8) and PMOS (MOSFET3-MOSFET4) differential pairs provide the negative resistance to cancel losses in the LC resonator. The respective transconductance of each pair was kept the same and the total negative trans-conductance became $-g_m$. As a result, less current was used and the loss of tank circuit was compensated, which led to lower power consumption.

For oscillation to occur, the g_m of each MOSFET must be:

$$g_m \geq \frac{RC}{L} \qquad (3)$$

Taking into consideration all the parasitic capacitance of the VCO MOSFETs, the frequency of oscillation can be derived as:

$$w_0 = \frac{1}{\sqrt[2]{L(C + C_{gs} + 4C_{gd_0})}} \sqrt[2]{1 - \frac{R^2(C + C_{gs} + 4C_{gd_0})}{L}} \qquad (4)$$

From this equation it can be clearly seen that the transistor capacitance, C, requires a decrease in C value compared to the ideal case for a given resonant frequency [7]. Real-world sources have unwanted amplitude or phase of the signal.

In 1966 Leeson [8] set up the following expression to measure phase noise more accurately. The phase noise of an LC-VCO can be described as in equation (5):

$$L(\omega_c, \Delta f) = 10 \log \left[\left(\frac{\omega_c}{2Q_L\, \Delta\omega} \right)^2 + 1 \right] \left(\frac{\Delta\omega 1/f^3}{\Delta\omega} + 1 \right) \left(2 \frac{FKT}{p_s} \right) \qquad (5)$$

where is the output frequency, is the loaded quality factor of the tank, is the angular frequency offset from the output frequency, *F* is the noise factor of the amplifier, $\Delta\omega 1/f^3$ is the flicker noise corner frequency, *k* is Boltzmann's constant, *T* is absolute temperature in Kelvin's, and P_s is the oscillator output power.

The quality factor (*Q*-factor) of the LC tank is determined by the *Q*-factors of the inductor and capacitor [9] as in equation 6:

$$\frac{1}{Q_{tank}} = \frac{1}{Q_c} + \frac{1}{Q_L} \qquad (6)$$

It can be shown that the oscillation frequency of an ideal tank with inductor L_1 and capacitor C_1 is given by:

$$f_0 = \frac{1}{2\pi \sqrt[2]{LC}} \qquad (7)$$

For a CMOS oscillator, the noise factor, *F* , can be expressed as:

$$F = 1 + \frac{K_1 \gamma I_{bias} R}{V} + K_2 \gamma g_{bias} R \qquad (8)$$

where K_1, K_2 are constant, γ is a FET noise factor, g_{bias} refers to the current source transconductance, R is the tank resistance, and *V* is the output voltage [9]. The phase noise of the oscillator could be reduced by increasing the amplitude of the output signal from Leeson.

The VCO is the more efficient if the oscillation amplitude for a given voltage supply is wider. It is noted that as the *Q* factor of the tank increases, phase noise decreases.

CMOS technologies are very attractive due to the high-level integration capability of both digital analogue blocks. However, standard CMOS processes suffer several drawbacks, such as high flicker noise and low breakdown voltage. As a result, they will directly affect and limit the obtainable phase noise performance of a VCO realized in CMOS.

In the CMOS process, transistor noise is generally high and causes serious degradation of VCO phase noise performance. However, the noise of PMOS is usually lower than NMOS by one order of magnitude [9]. Moreover, the measured minimum noise figure of NMOS and PMOS transistors under exact bias level also shows clearly PMOS is lower than that of the NMOS.

III. Simulation Results

Circuit simulation has been conducted by Agilent ADS simulation tool, the Advanced Design System that is the world's leading electronic design automation software for RF, microwave, and high-speed digital applications, produced by Agilent Technologies Inc**.**

The circuit generates stable periodic outputs, as shown in Fig. 2 and Fig. 3 respectively, with a harmonic index as shown in Fig. 4.

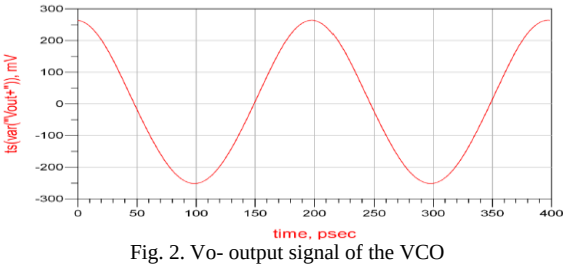

Fig. 2. Vo- output signal of the VCO

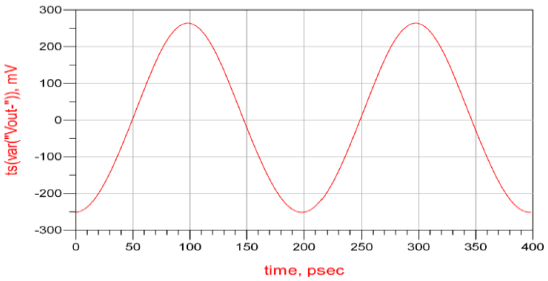

Fig. 3. Vo+ output signal of the VCO

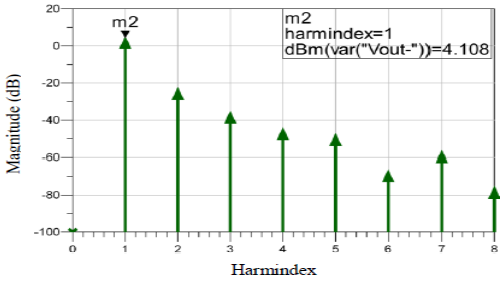

Fig. 4. Harmonic index of the VCO

The phase noise was measured versus frequency. The phase noise improves as the varactor gain decreases. Therefore, the worst phase noise is recorded. The phase noise of -133.07 dBc/Hz and -136.31 dBc/Hz at 600 kHz and 1 MHz frequency offset are obtained at 5.0 GHz frequency, as shown in Fig. 5 and Fig. 6 respectively.

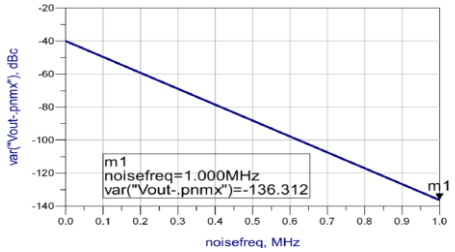

Fig. 5. Simulated phase noise at 1 MHz offset

The power consumption of this VCO is inversely proportional to its phase noise [7]. Phase noise versus supply voltage is shown in Fig. 7.

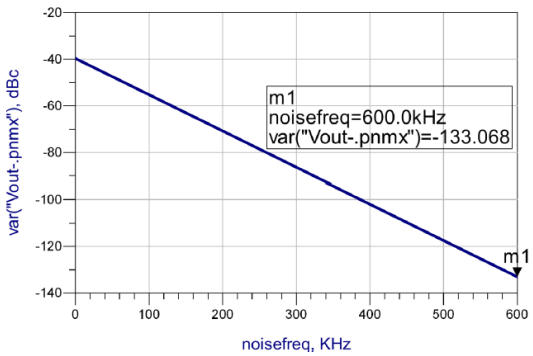

Fig. 6. Simulated phase noise at 600 kHz offset

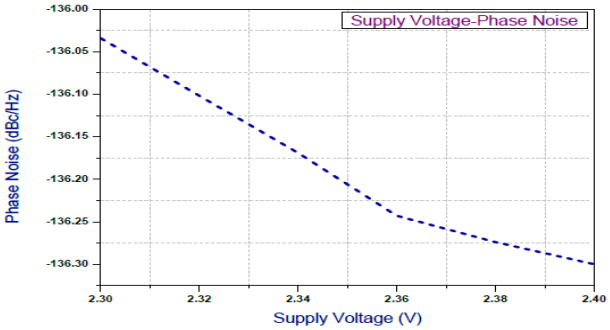

Fig. 7. VCO phase noise at 1 MHz offset frequency versus supply voltage

To compare the performance of previously published oscillators, and FOM, the one we have used and widely accepted was adopted by Ham and Hajimiri [10], and it normalizes the measured phase noise with respect to center frequency and power consumption. It is defined by equation (9):

$$FOM = L(f_0, \Delta f) + 10\log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{P_d}{1mW}\right] \quad (9)$$

where $L(f_0, \Delta f)$ is the phase noise at Δf offset frequency, f_0 is the oscillating frequency, and P_d (W) is the power dissipation of the VCO.

The phase noise is automatically decreased while the power consumption is reduced [11]. So there is a trade-off between the power consumption and phase noise. An optimization technique is used to design the FOM.

The major losses being assumed are those associated with the series resistance of the resonator inductor. The results obtained from the simulation of the LC-VCO design show that the phase noise has been drastically reduced, as illustrated in Table I.

TABLE I: Summary of Measured Results

Resonant Frequency, f_0 (GHz)	5.00
Supply Voltage (V)	2.40
Power Consumption (mW)	2.45
Tuning Range (GHz)	4.62-5.51
Tuning Voltage (V)	0.0-2.0
Phase Noise (dBc/Hz)	-133.70@600kHz offset.
	-136.31@1MHz offset
FOM (dBc/Hz)	206.20

Table II summarized measurement and compares to those recently published CMOS VCOs, it is observed that the proposed VCO exhibits comparable circuit performance

under low dc-power consumption.

TABLE II: SUMMARY OF MEASUREMENT RESULTS AND PREVIOUSLY REPORTED VCOS, USING CMOS

Process	Freq (GHz)	Power (mW)	PN (dBc/Hz)	Offset (MHz)	FOM (dBc/Hz)	Ref.
0.18μmCMOS	5.46	6.40	-100.30	0.1	-187.00	[12]
0.18μmCMOS	5.20	9.70	-113.70	1.0	-180.00	[13]
0.18μmCMOS	5.00	1.10	-117.70	1.0	-191.80	[14]
0.18μmCMOS	5.80	10.80	-117.00	1.0	-184.00	[15]
0.35μmCMOS	2.80	6.30	-121.00	0.6	186.30	[16]
0.35μmCMOS	5.00	2.40	-136.31	1.0	-206.20	This Work

The design of the proposed VCO proved to be best performance. The phase noise is also considerably very good where the FOM is found to be excellent.

IV. CONCLUSIONS

This paper presents a novel 5.0 GHz LC-VCO architecture that can achieve low phase noise based on cross-coupled topology in a 0.35μm CMOS technology. The phase noise of the oscillator was optimized and the measured worst-case phase noise is -133.07 dBc/Hz and -136.31 dBc/Hz at 600 kHz and 1 MHz frequency offset, respectively. As a result, this CMOS VCO achieves the best FOM of -206.20 dB with approximately 17.8% tuning range. This work can be extended in several other dimensions such as the tuning range chip area and as performance indices for optimization.

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H. Zhirun received his BEng in Telecommunication Engineering from Nanjing University of Posts and Telecommunications, Nanjing, China, in 1982; and Master in Business Administration, and PhD in Electrical and Electronic Engineering from the Queen's University of Belfast, United Kingdom, in 1988 and 1991, respectively. His main research interests are in RF/microwave/millimetre-wave device, circuit and antenna modelling, optimization, design, realization and characterization. He has published more than 100 peer-reviewed journal and conference papers.

M. A. Aqeeli received his Bachelor of Science (BS) in Electronic and Communication Engineering from King Abdul Aziz University, Jeddah, Saudi Arabia, in 1991; and Master of Science (MS) in Electronics Instrumentation Systems, University of Manchester, Manchester, England, in 2005. He has 15 years' experience as director of the Precision Measurement Electronic Laboratory (PMEL) of Royal Saudi Air Defence Forces (RSADF). He attended more than 14 training courses in Uncertainty Calculation, Traceability of Measurements, Calibration Laboratory Management, Measurement of Uncertainty-Measurement Assurance, Quality Metrology Systems in the USA and Europe, and is currently working towards a PhD degree at the School of Electrical and Electronic Engineering, University of Manchester. His research interests include RF/microwave devices, tracking signal generators, and oscillators.