Design and Optimization of CMOS 0.18μm Low Noise Amplifier for Wireless Applications

V. P. Bhale and U. D. Dalal

***Abstract*—A design and optimization of 3 GHz single ended Radio Frequency (RF) Low Noise Amplifier(LNA) for wireless applications using standard UMC 0.18μm CMOS technology is reported. Designing of RF circuit components is a challenging job, since even after performing lengthy calculations and finding parameter values it is less guarantee that the design performs as expected. In view of this the optimization tool; Elitist Non-Dominated Sorting Genetic Algorithm (NSGA-II); has been employed to get the optimized starting values of components in the design. The obtained NSGA-II parameters were simulated using Cadence Spectre-RF simulator. The designed Low Noise Amplifier achieves a power gain of 14.49 dB and a minimum Noise Figure of 1.897 dB is achieved. It dissipates 11.7 mW of power out of 1.8 V supply.**

***Index Terms*—NSGA-II algorithm, LNA, noise figure, power gain.**

I. Introduction

The growth of multimedia services and applications in digital data transmission has led to ever increasing demands of wireless communication systems [1]. New standards are being approved and designed in order to tap the exploding market, many of these new standards attempt to connect devices and or appliances in the home using lower performance radio transceivers. Also, recent years have experienced explosive growth in the Radio Frequency /microwave semiconductor industry owing to the proliferation of a host of applications. Single-chip Bluetooth devices are already available and similar integration is likely to be achieved in cellular telephones and wireless networking in near future.

Radio Frequency components are the basic building blocks of transceivers operating in GHz frequency range. Designing of RF circuit component needs lot of effort. After performing lengthy calculations and finding the parameter values it is not guaranteed that the circuit performs as expected. In Radio Frequency Integrated Circuits (RFIC), Low Noise Amplifiers are considered as black magic box because of their uncertain response with higher frequencies. Due to mismatch of input impedance and output impedance maximum power transformation is not possible. For Designing of the tank circuit, input and output impedance circuit, we need to design a passive filter with optimized component values. Optimization of the component value is a time consuming job. In view of this a CAD tool using Non-Dominated Sorting Genetic Algorithm (NSGA-II) has been employed. The design goal is formulated as an objective function. Some approximations and estimations on the design parameters are made in order to satisfy the requirement of the genetic algorithm. Many applications of genetic algorithm and optimization of LNA parameter by binary coded genetic algorithm is reported in [2], [3]. In this paper we are presenting optimization for single ended LNA using real coded genetic algorithm. In Section II; brief introduction of Non-Dominated Sorting Genetic Algorithm is given. In Section III analysis and design problem of low noise amplifier is presented, in Section IV design objective and constrains optimization of LNA is mentioned. In Section V simulation result and discussion is presented. Scope and limitation of the NSGA-II has been discussed in Section VI and finally Section VII concludes the paper.

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II. Elitist Non-Dominated Sorting Genetic Algorithm (NSGA-II)

Genetic algorithms [3], [4] are search techniques used in computing to find true or approximate solutions to search or optimization problems. It is based on concepts of natural selection, reproduction and mutation and has been used extensively in optimization problems. It can be classified in two sets depending on type of coding of the members; one is binary coded and second is real coded [3].

In past few years GA has undergone lots of developments developing its features, processing time etc, some such developments are Multi Objective Genetic Algorithm (MOGA) [5], [6], Elitist Non Dominated Sorting Genetic Algorithm [3].

III. Analysis and Design of Low Noise Amplifier

The early part of this section is based on the literature survey and concludes with own design. As one of the essential components, Low Noise Amplifiers (LNAs) for wireless applications have attracted significant research interest and various approaches to the design of narrowband LNAs (operating below 3 GHz) and wideband LNAs (operating above 3 GHz) have been proposed previously [7]-[15] and as shown in Fig. 1(a)- Fig. 1(d). Distributed amplifiers [7] can provide very large bandwidth because of their unique gain-bandwidth trade-off. However, large power consumption and chip area make them unsuitable for typical low –power, low cost wireless applications. Common-gate amplifiers [8], [9] exhibit excellent wide band input matching, but suffer from a relatively large noise figure (NF). Narrow-band LNAs like an inductively degenerated common-source amplifier can also be converted into a wideband one by adding a wideband input matching network

[10]. However, the insertion loss of the passive input matching degrades the NF rapidly with frequency. Resistive-feedback amplifiers [11]-[14] have very good wideband input matching characteristics. However, low NF and low power consumption can be hardly achieved simultaneously across a large frequency range. In [15], noise cancellation technique is used to relax this trade-off in resistive feed-back amplifiers.

A typical LNA must fulfill several challenging requirements. The LNA must provide a good input matching over a band more than 500 MHz. A high gain is also preferred to amplify the week signals at the receiver and to overcome the noise effects from the subsequent stages. In addition, the noise figure of the LNA must be low (< 3 dB) since it plays a major role in defining the receiver's sensitivity. Moreover, the LNA also has to be power efficient and physically small to save power and reduce the cost, respectively.

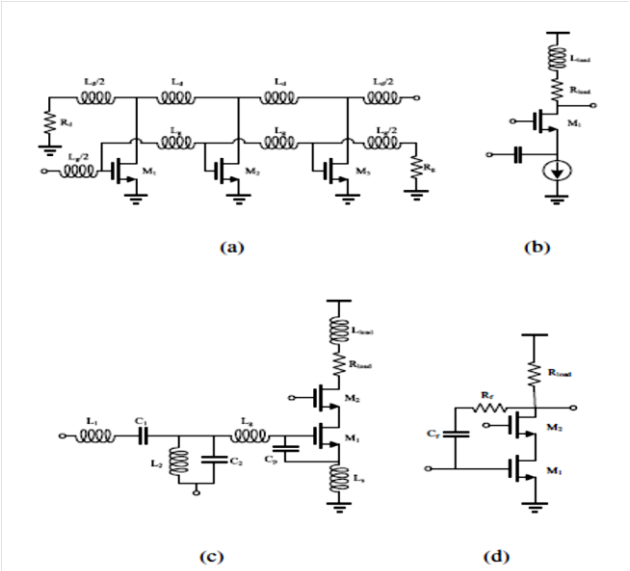

Fig. 1. Various LNA topologies (a) distribute amplifier, (b) common gate, (c) inductive degeneration, (d) resistive feedback.

Using the available literature as references, the specific goal here is to achieve a low-power (<11 mW) operation, medium gain (power gain >10 dB) LNA, a small noise figure (<2.5 dB). An inductively degenerated LNA configuration is proposed, as shown in Fig. 2(a).

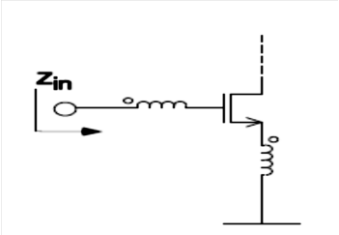

Fig. 2(a). Inductive source degeneration.

Inductive degeneration improves the linearity of the amplifier. The input impedance can be derived from the small signal analysis [16] of Fig. 2(b). By looking into the input side of Fig. 2(b), input impedance Z_{in} can be:

$$Z_{in} = s(L_s + L_g) + R_g + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s \quad (1)$$

where L_s, L_g are the source and gate inductances, respectively; R_g is the transistor gate resistance, C_{gs} is the transistor gate-to-source capacitance; g_m is the transistor trans-conductance. The inductor parasitic resistance is ignored here. Input match requires that at the resonance frequency of the circuit, the impedance of the input stage is purely real and should be equal to 50Ω.

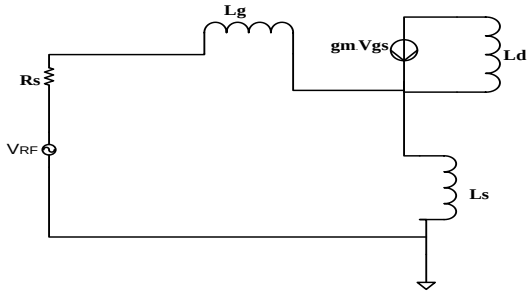

Fig. 2(b). Small signal equivalent of Fig. 2(a).

It follows that:

$$R_g + (\frac{g_m}{C_{gs}})L_s = 50 \quad (2)$$

where ω_0 is the resonance frequency (rad/s), and

$$j\omega_0(L_s + L_g) + \frac{1}{j\omega_0 C_{gs}} = 0 \quad (3)$$

The noise factor (F) is defined as [7], [8]:

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} g_m R_s (\frac{\omega_0}{\omega_T})^2 \quad (4)$$

$$NF = 10 \cdot \log_{10}(F)$$

where unity frequency:

$$\omega_T = \frac{g_m}{C_{gs}}, \ \alpha \equiv \frac{g_m}{g_{d0}},$$

R_s: source resistance, R_l: series resistance of inductors, R_g: gate resistance, γ: the thermal noise coefficient, ω_0 : the resonance frequency, g_m: transistor trans-conductance.

For a source inductively degenerated LNA in Fig. 2, we could put a lower bound on the trans-conductance of the input transistor to ensure that the final designed LNA can provide a reasonable gain [9] .

$$A_V = G_m Z_{eq} = \left(\frac{1}{jw_0 L_s}\right)\left(\frac{jw_0 L_1}{1 - w_0^2 L_1 C_0}\right) \quad (5)$$

In order to formulate a geometric programming problem, we have to do some transformation and introduce new variable to satisfy the requirement of geometric programming on the objective and constrains. Inequality constrains and the objective function must be in the form of polynomial, equality constrains must be in the form of monomial. Here noise figure and gain is formulated for low noise amplifier.

For low noise amplifier, Objective function of Noise Figure can be formulated as:

$$F = F_{\min} + 50 \times R_n \times \left(0.02 - G_{opt}\right)^2 \quad (6)$$

where, $F_{\min} = \dfrac{1+2\times W_0 \times \sqrt{\delta \times \gamma \times (1-C^2)}}{Wt \times \sqrt{5}}$

$$Rn = \frac{\gamma}{\alpha \times G_m}$$

$$Gopt = \alpha \times W_0 \times Cgs \frac{\sqrt{\delta \times (1-C^2)}}{5 \times \gamma}$$

Objective function of the Gain of LNA can be formulated as:

$$Gain = \frac{W_t \times R_{load}}{W_0 \times 2 \times R_{load}} \quad (7)$$

And objective function of power consumption has been formulated as:

$$P_{DC} = I_D \times V_{DC} \quad (8)$$

where,

$$I_D = \frac{\mu_n \times C_{ox} \times Width \times V_{od}^{\ 2}}{2 \times ChannelLength}.$$

In above equation second order effects on drain current have been neglected to reduce the complexity of the program. As the schematic diagram of the LNA is depicted in Fig. 3, an input impedance matching circuit is needed to match source impedance to transistor input impedance.

Objective function for Input impedance can be formulated from following equation.

$$Z_{in} = s(L_s + L_g) + R_g + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s \quad (9)$$

L_s and L_g is used to tune the input impedance (Z_{in}) to $50\,\Omega$ at 3 GHz frequencies. C_{gs} and R_g Model the impedance looking into the gate of MOSFET. Here we can include pad capacitance and bond wire inductance also [10].

IV. Design Objectives and Constraint Optimizations for NSGA-II

The simulations have been done for LNA with following constraints. Based on the technology parameters following have been defined as constant:

$$Cox(fF/\mu m2) = 8.632, Rs(\Omega) = 50, RL(\Omega) = 50,$$
$$\beta(\Omega/nH) = 1, \gamma = 2.5, L(\mu m) = 0.18, \lambda = 0.5,$$
$$Vth = 0.47V, Vdd = 1.8V$$

Design constraints for the component of circuit were taken as follows:

1) $5 \le W1 \le 105\,\mu m$ 2) $0.1 \le Ls \le 50nH$

3) $0.1 \le Lg \le 50nH$ 4) $0.1 \le C \le 0.5\,pF$

Simulations have been done with these parameters using NSGA-II. The NSGA parameters that were given are as follows: Mutation probability= 0.23671, Population size=100, Crossover Probability=0.99431, Number of generations=50.

V. Simulation Results and Discussions

A. Simulation Results Using NSGA-II

The above mentioned optimization technique is implemented for Low Noise Amplifier design to optimize gain and noise figure. Direct equations have been used for gain and noise figure which were calculated for cascode LNA with inductive source degeneration. Program structure for LNA optimization using NSGA-II is shown in Fig. 3 below.

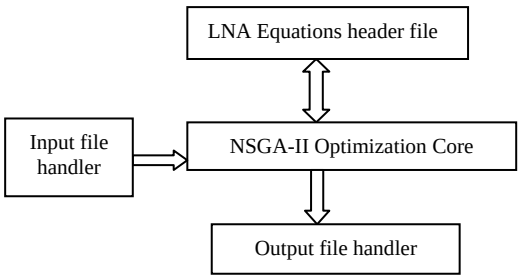

Fig. 3. LNA optimization program structure.

The "func-con.h" header file has been modified and the fitness functions and constraint functions have been replaced with the equations as discussed in Section III. Also, "LNA_equations.h" file has been added, which actually evaluates all these equations. After NSGA-II optimizer generates output files, another program converts those into design parameters and we can plot those values using GNUPLOT software as plotted in Fig. 4(a)- Fig. 4(f)

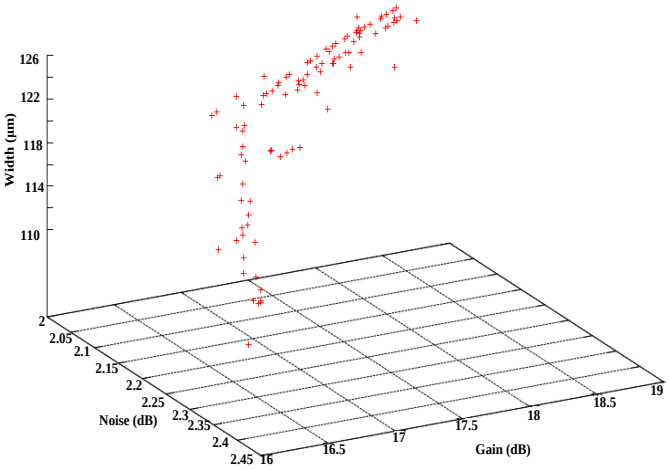

Fig. 4(a). Noise *vs*. gain *vs*. width of the transistor.

The trans-conductance, g_m, of the device is very much important to achieve good gain for LNA. However, this g_m depends on the transistor width. Also g_m/I_D ratio needs to be maintained to achieve a required LNA gain. Thus, the width of the transistor needs to be chosen to give enough gain and minimum noise figure. From Fig. 4(a), thus, 'W' is chosen to be 105 μm.

The overdrive voltage is one of the important parameter for transistor operating point analysis. The transistor should operate in desired operating region for maximum gain. Thus plots in Fig. 4(b) are plotted using NSGA-II to guess the initial overdrive voltage required for the transistor to be in desired operating region. The V_{od} is chosen to be 0.35V.

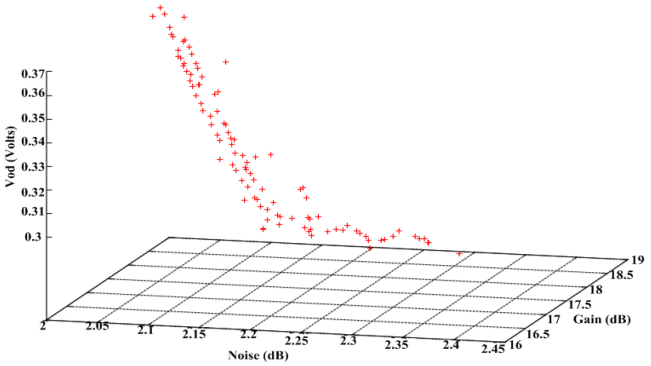

Fig. 4(b). Noise *vs*. gain *vs*. overdrive voltage.

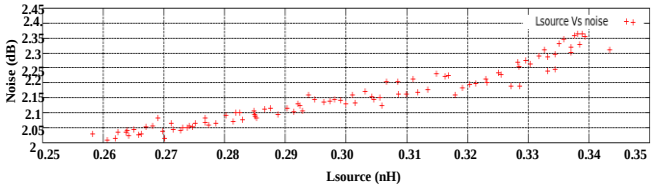

Fig. 4(c). Noise *vs*. lsource.

The role of source degenerated inductor here is to match the input impedance to 50Ω with low noise. From Fig.4(c), it can be seen that the noise is increasing with L_{source} .Thus the optimum value of L_{source} at minimum noise figure is chosen to be 0.27nH.

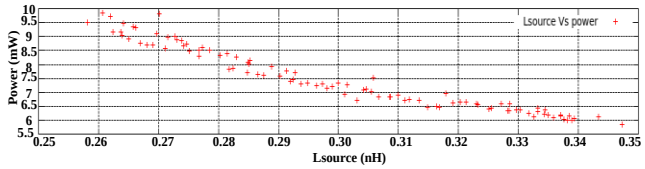

Fig. 4(d). Power dissipation *vs*. lsource.

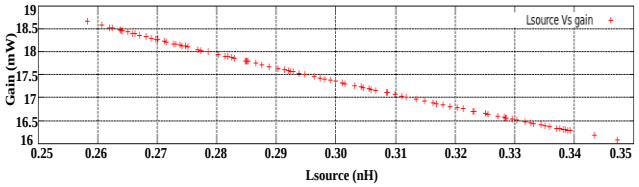

Fig. 4(e). Gain *vs*. lsource.

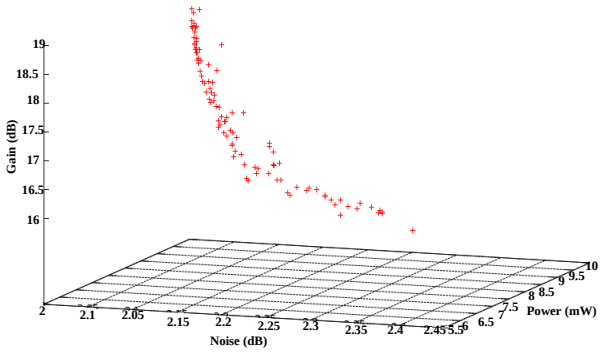

Fig. 4(f). Power *vs*. noise *vs*. gain.

The effect of variation of source inductor on power consumption can be seen from Fig. 4(d), where it can be seen that with the increase in value of inductor power dissipation reduces. But, for RF design the inductor should not be bulky. While, from Fig. 4(e), it can be seen that the gain reduces with the increase in value of the source degenerated inductance .Thus, L_{source} =0.2nH has been chosen as optimum value which gives best compromise between gain and noise figure trade-off.

There always exists a trade-off among power dissipation, gain and noise figure for a Low Noise Amplifier design. The same can be seen in Fig. 4(f).

B. Simulation of LNA Using Spectre RF

The initial start up values given after running NSGA-II algorithm has been used for the designing of CMOS Low Noise Amplifier for 0.18 µm technology. The design is finally simulated using Cadence Spectre design tool. Fig. 5 shows the schematic entry for the same in Cadence Spectre RF tool. The S-parameter analysis is performed to obtain the gain and noise figure parameters. Also parallel LC tank circuit at the output tunes to the operating frequency of 3GHz.Capacitors at the input and output are dc blocking capacitor. The source terminal inductor needs to be properly design to have a 50Ω input matching. The dc blocking capacitors has been chosen to be of 103fF each. While L_g is calculated from Eq(13), once the optimum value of L_s is chosen to be 0.27nH.Usually value of L_d is picked up from the available literature as references and accordingly the parallel tuning capacitor needs to be tune to operate at 3 GHz frequency. The value of bias resistor, R_{bias}, is chosen to be large to minimize the noise entering into the design.

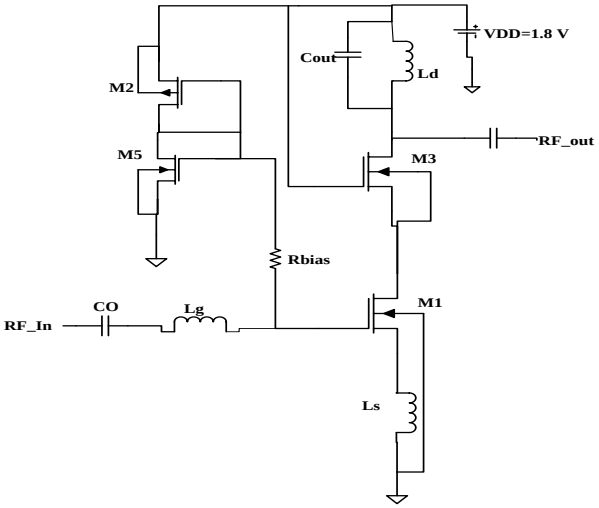

Fig. 5. Designed single ended LNA using Spectre RF.

Therefore, R_{bias}=10 K has been chosen as optimum value. The width of the current mirror transistor, M5, should be same as that of the cascode transistor, M1 i.e.105µm. Table I shows the simulation results for the single balanced low noise amplifier using NSGA-II optimization algorithm. The operating frequency is 3 GHz for Wide Band Wireless application. These design parameters are used to build a circuit and it was simulated with Cadence RF Specter design tool. Single ended Low noise amplifier has been designed with obtained parameters for frequency of 3 GHz and Channel Length = 0.180 µm. The values were taken after running GA for 50 generations. For LNA, values are as follows: *Ls* = 0.27 nH, *Lg* =2.00 nH, *Co* = 103fF, W_1 = 105um. From Fig. 6, the design achieves 14.49 dB gain and 2.481dB of overall noise figure and 1.897 dB of minimum noise figure, respectively, shown in Fig. 8 and Fig. 7.

At the time of designing parasitic play important role in

obtained results but here we are not considering them because our first motivation is to take initial guess of the values. The design parameters obtained from multi objective genetic algorithm is comparable with the result obtained in Cadence Spectre tool.

TABLE I: OPTIMIZED RESULTS FOR LOW NOISE AMPLIFIER WITH NSGA-II

Parameters	Targeted Specifications	Optimization with NSGAII
Operating Frequency	3 GHz	3 GHz
Technology	CMOS 180nm	CMOS 180nm
Supply Voltage	1.8V	1.8V
Gain, S_{21}	≥14dB	14.49 dB
Noise Figure, NF	<3dB	2.481dB
Minimum Noise Figure, NF_{min}	<2.5dB	1.897db
Power Dissipation (mW)	≤11mW	11mW

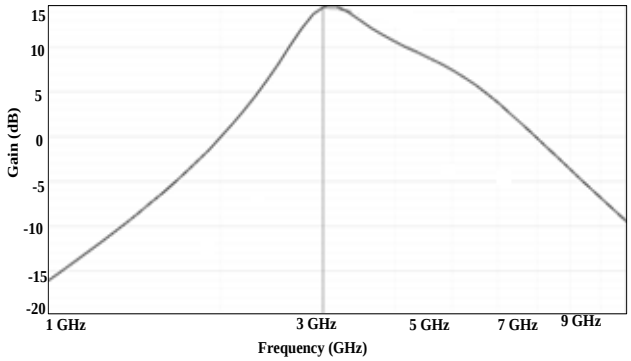

Fig. 6. Gain *vs*. frequency obtained by Spectre RF simulation for LNA.

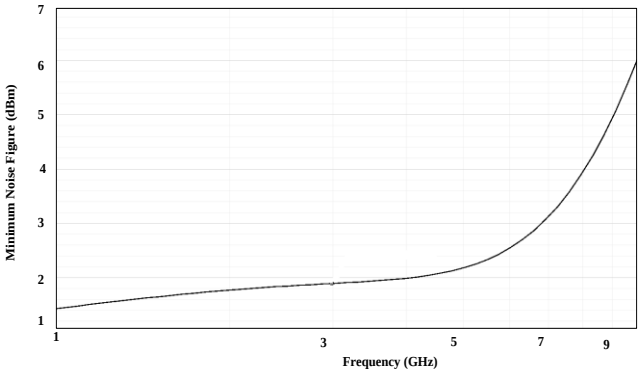

Fig. 7. Minimum noise figure *vs*. frequency obtained by Spectre simulation.

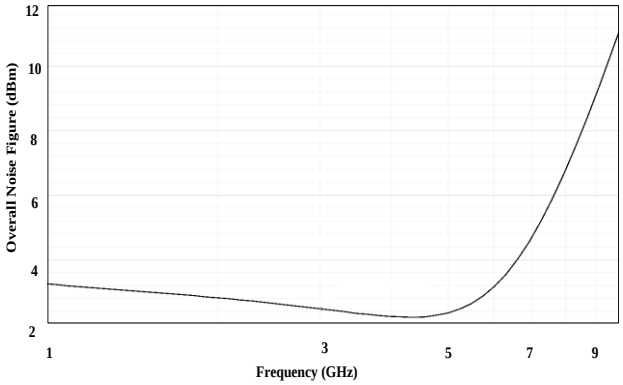

Fig. 8. Overall noise figure *vs*. Frequency obtained by Cadence Spectre simulation.

VI. SCOPE AND LIMITATION OF DESIGNED TOOL

Designed optimization tool gives only approximate values of the design parameters. This tool is designed only for final stages of RFIC design process. Parasitic effects associated with passive on-chip components like capacitors, inductors and resistors have not been taken into account for shorter simulation time of the circuit.

VII. CONCLUSION

This paper shows that the optimization of RF Circuits is possible with real coded genetic algorithm. It is found that real coded Multi-Objective Genetic Algorithm has many advantages over binary coded genetic algorithm. Non-Dominated Sorting Genetic Algorithm is used for optimization tool, which is giving comparative results with design software simulation like Cadence Spectre tool. In this paper it is shown that the Low Noise Amplifier can be designed for parameter for noise figure of 1.897dB and power gain of 14.49dB.In future the NSGA-II optimization tool can be used to extend for 3-5GHz LNA design for wideband wireless RF system. Thus the design tool is useful in finding circuit element values quickly reducing the RF circuit designer time.

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