A 12Bit 200Msps Spilt-Based Pipeline ADC Design

Haijun Lin, Hao San, and Ye Tian

***Abstract*—This paper presents a 12bit 200Msps pipeline ADC fabricated in TSMC 0.18um CMOS technology. For high resolution pipeline ADC design, the operation speed is limited by sampling capacitance load of OTA inside the ADC. The proposed ADC is realized in split-based pipeline architecture, sampling capacitance of ADC is separated into two channels. Each channel only has half capacitance, which reduce capacitive loading of OTAs in each channel and realize high speed operation of the ADC. The ADC achieves an SNDR of 64.7dB, SFDR of 86.3dB with analog input frequency of 10MHz, sampling frequency of 100MHz and differential amplitude of 1.25Vpp without digital calibration. The power dissipation of ADC is 356mW at 1.8V supply.**

***Index Terms*—OTA, pipeline ADC, split-based.**

I. Introduction

CMOS ADCs with sampling rate more than 100Msps and resolution more than 10bit are widely used in optical communication system, wireless and wired broadband communication systems [1]. Pipeline is the appropriate architecture widely used in this class of ADCs for its reasonable trade-offs among sampling rate, resolution and power. To realize the high sampling rate and high resolution pipeline ADC, the OTA to drive large sampling capacitance inside MDAC becomes the bottleneck which limits the sampling rate of ADC. Split ADC architecture is the useful method to reduce the capacitance need to be driven by OTA in pipeline ADC [2]. Split-based pipeline ADC consists of 2 independent ADCs with the same circuit structure which shares a same SHA [3]. The block diagram of traditional split ADC is shown in Fig. 1, The output code of ADC (A) and ADC(B) are X_A and X_B respectively. By average calculation, the final output code of the ADC can be written as Eq. 1, and difference between outputs of 2 ADCs can be written as Eq. 2.

$$X = \frac{X_A + X_B}{2} \tag{1}$$

$$\Delta X = X_B - X_A \tag{2}$$

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In Eq. 2, $\triangle X$ is the output of two channel ADC difference due to mismatch between two ADCs. This value can be used to calibrate the channel mismatch such as capacitance mismatch and OTA gain mismatch between ADC (A) and ADC (B).

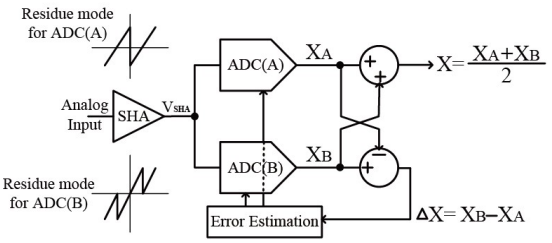

Fig. 1. The traditional split ADC block diagram.

Several digital calibration algorithms for split ADC are proposed [1]-[6]. But for high speed pipeline ADC design, the digital calibration for split ADC has three difficulties:

1) In Fig. 1, the residue transfer curve is different between two ADCs. Which means the different reference voltage is required for two ADCs for calibration.
2) In Fig. 2, random sequences should be injected to ADC. q_{1A}, q_{1B}, q_{2A}, q_{2B} are examples of random sequence injected to ADC. Calibration time is very long, which limits ADC production throughput, the reliability of the random sequences injection is not proved by industry [5].
3) In Fig. 2, while random sequences are injected to ADCs for $_{\text{calibration}}$, extra switches should be added into signal paths, the additional switch ON resistance increases RC time constant in signal path, which will decrease the operation speed of ADC.

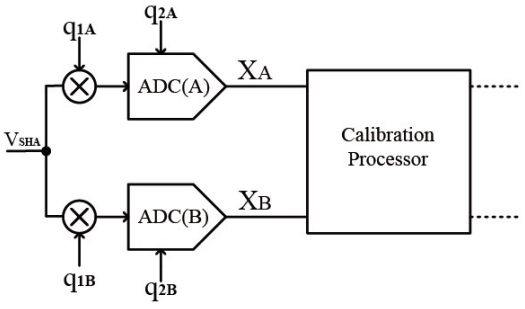

Fig. 2. Example of split ADC with random sequence.

Split ADC is not be used for high speed ADC for difficulties discussed above. To apply this architecture on high speed ADC, split-based pipeline ADC without digital calibration is proposed, no extra switches in signal paths, OTAs in each ADC only drive half capacitance, which relax design requirement of OTAs and increase the operation speed of ADC. Since only one SHA used for two channel ADCs,

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clock mismatch between channels need not be considered. The proposed split-based pipeline ADC operates with sampling frequency of 200MHz and resolution of 12bit can be confirmed.

The architecture of proposed split-based pipeline ADC is discussed in Section II. The circuit design is introduced in Section III. Measurement results are discussed in Section IV and Section V summarizes and concludes this paper.

II. Architecture of Proposed ADC

Traditional 12bit pipeline ADC is shown in Fig. 3 [7], which is composed of five 2.5 bit stages and a 2bit flash converter. In Fig. 3, V_{inp} and V_{inn} are analog input differential signals of ADC. To realize resolution of 12bit and sampling frequency of 200MHz, from calculation and simulation, the design requirement of OTAs in each 2.5bit sub-ADC stages is shown in Table I.

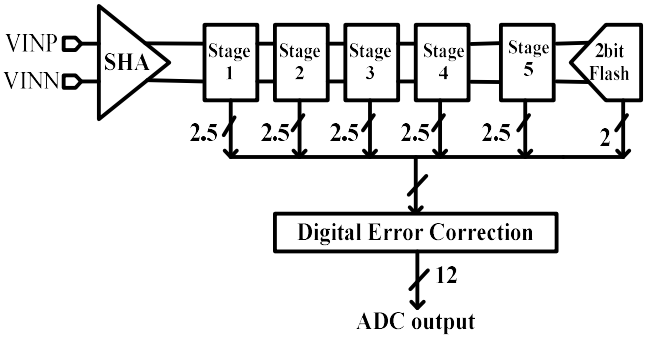


Fig. 3. Traditional 12bit Pipeline ADC architecture.

TABLE I: Design Requirement of OTA in each Sub-ADC Stage

Parameters	OTA1	OTA2	OTA3	OTA4	OTA5
DC gain (dB)	78	68	56	44	32
GBW (GHz)	3.7	3.2	2.6	2.1	1.6
Load (pF)	2	0.75	0.38	0.18	0.05

From Table I, it is clear that the design requirements on OTAs in each stage are very rigor. The operation speed of OTA is depends on sampling capacitance be driven by OTA. Large output current from OTA is required to drive large sampling capacitance for high speed operation, which increases power dissipation. In order to realize high gain of OTA, large g_m, hence large W/L is required. However, the large gate parasitic capacitor of MOSFET at input of OTA will limit the sampling speed of ADC. To realize high speed sampling, split-based pipeline ADC is proposed.

Fig. 4 shows the basic idea of split-based ADC, Fig. 4 (a) shows an N bit ADC with single channel, g_m means the transconductance of OTA and C means the total capacitance, the last block means the digital circuit in ADC. Because the bandwidth f_T of the OTA is proportional to g_m/C, power P is proportional to g_m. In the other hand, in a split based ADC (Fig. 4 (b)), OTAs in each ADC channel has half g_m, half load and the half power with the same bandwidth, thermal noise will increase 3dB in each channel since capacitance is half compared with the single ADC. However, since output of two channel ADCs be averaged, increased noise is recovered in the output. The digital output D_{out} can be written as $D_{out}=(D_{out}(A)+D_{out}(B))/2$. As the result, the bandwidth, noise level, and total power of split ADC is the same as the single ADC.

The proposed spilt-based pipeline ADC is shown in Fig. 5. The ADC (A) and ADC(B) are the same ADC with five 2.5bit sub-ADCs and a 3bit flash ADC for considering linearity, maximum conversion rate, power consumption and chip area. Redundancy correction of sub-ADC output code and average calculation of two channel ADCs are processed with on-chip digital block. Digital calibration is not used in proposed spilt-based pipeline ADC for problems of calibration time and operation speed.

The split-based pipeline ADC relaxes the design requirement on each ADC especially for OTA, so that this architecture is suitable for high speed high resolution pipeline ADC implementation. Compared to time interleaved ADC, split-based ADC uses a single SHA to eliminate the effect of sampling phase inaccuracy among each ADC channels. Also this proposed architecture can be expanded to four channels and more than four channels application.

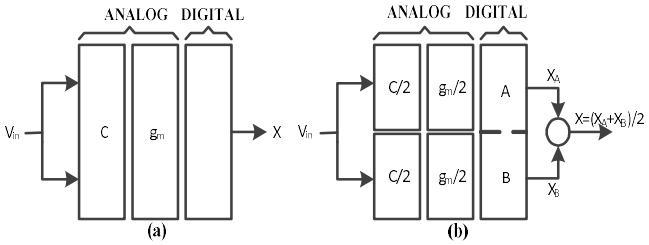


Fig. 4. Principle of split-based ADC.

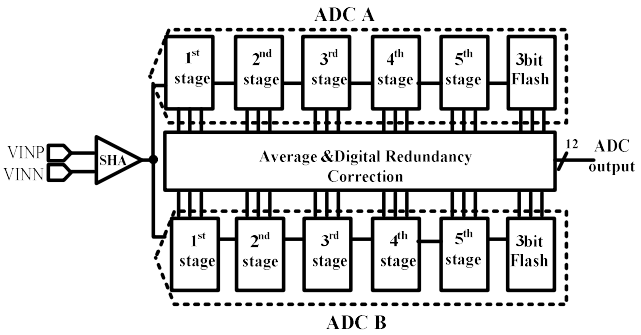


Fig. 5. Proposed split-based ADC architecture.

III. Circuit Implementation

The proposed split-base 12bit 200Msps pipeline ADC is composed of SHA, split-based ADC, band-gap circuit, reference generator, DLL, clock distribution circuit, LVDS and digital control circuit. The block diagram of proposed ADC is shown in Fig. 6.

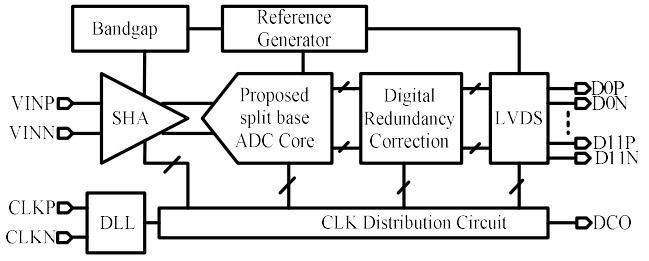


Fig. 6. The Block Diagram of Proposed ADC.

SHA is used to sample and hold input analog signal, band-gap circuit generates reference signal and common mode signal of system, reference generator makes reference signal of comparator of ADC, DLL generates stable clock signals to ADC, Clock distribution circuit builds clock signals required by SHA, proposed ADC core, digital redundancy correction, LVDS. LVDS drives 12 bit digital output data (from D_{0p} to D_{11N}). DCO is the output clock used for output data capture.

In this section, the design of SHA and 2.5 bit ADC stage are introduced.

A. SHA

Sampling and hold amplifier (SHA) is the crucial part in a high speed and high resolution ADC, ADC performance such as dynamic range, distortion, SFDR and noise are largely dependent on SHA. In our implementation, wide band and low noise, high linearity SHA is required. The conventional two-capacitor flip around SHA architecture is appropriate selection. Fig. 7 shows the block diagram of the SHA. To reduce the charge injection and clock feed-through effect, bottom plate sampling technique is used. Sampling capacitor C_s is 4pF considering the required 12bit accuracy and kT/C noise at $1.25V_{p-p}$ full scale input, total capacitors for differential SHA is 4pF. The total capacitive load of SHA is sampling capacitors in 1st stage of two channel ADCs.

To reduce the ON resistance and nonlinearity of switches, S_1, S_2, S_{1a} are chosen as bootstrapped switches.

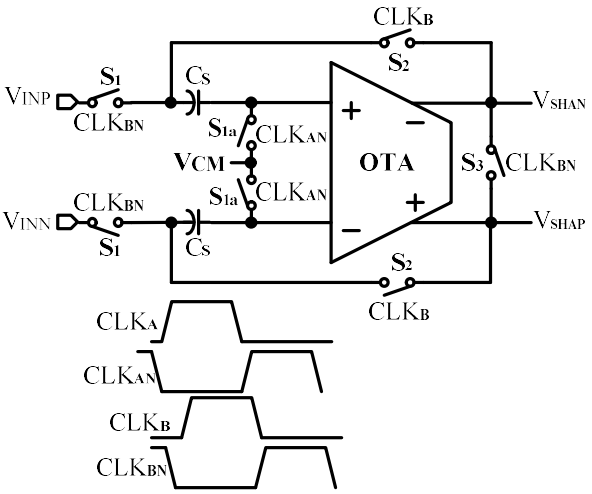


Fig. 7. Block diagram of SHA.

Clocks timing of SHA shows in Fig. 7, the rise edge of CLK_{BN} is the sampling phase and the fall edge of CLKB is the holding phase of SHA respectively.

Achieving sufficient dc gain at a high sampling rate with low power is a difficult challenge for OTA design. Although a multistage OTA offers high open-loop gain, the requirement of frequency compensation increases the OTA power. Single stage OTA offers large gain-bandwidth products with limited dc gain. To realize high gain, wide bandwidth and high drive capability, two-stage amplifier with gain boost folded-cascode architecture is employed. Fig. 8 shows the OTA circuit, the input stage is designed by PMOS, which induces thermal noise. Switched-capacitor common mode feedback is used to stabilize the common mode voltage.

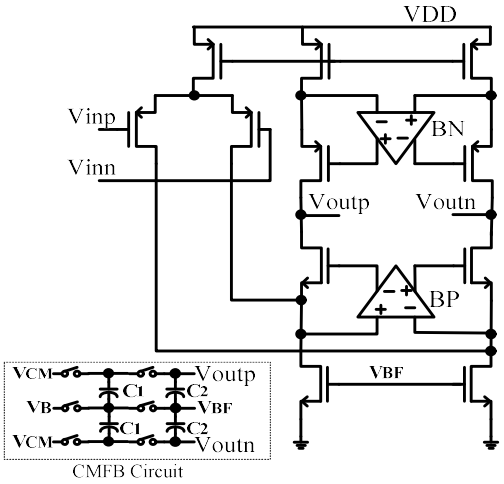


Fig. 8. OTA circuit used in SHA.

Simulated performance results of the OTA show in Table II.

TABLE II: SIMULATION RESULTS OF OTA IN SHA

Parameters	Input swing	CM Voltage	DC gain	GBW	SFDR
Value	$1.25V_{p-p}$	0.9V	79dB	1GHz	88dB

B. Pipeline Stage with 2.5bit MDAC

The proposed split-based pipeline ADC is implemented by 2.5bit MDAC, which includes six comparators, four switched capacitor circuit paths to realize charge calculation. The single-ended diagram of the 1st stage 2.5bit MDAC shows in Fig. 9.

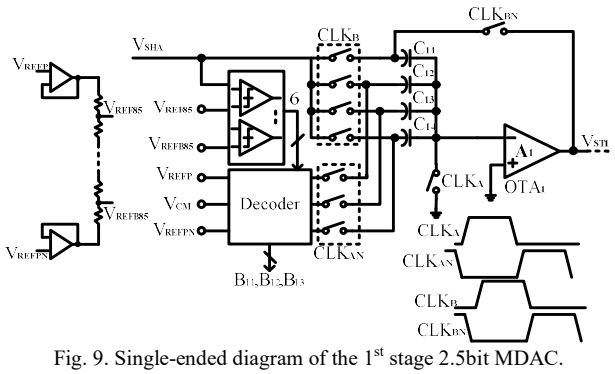


Fig. 9. Single-ended diagram of the 1st stage 2.5bit MDAC.

V_{SHA} is the input signal of 1st stage MDAC, which is the output of SHA, V_{REFP} and V_{REFN} are positive and negative reference voltage respectively and are created by reference generator, and reference voltage such as V_{REF85} and V_{REFB85} are reference voltage for comparators, which are created by resistor ladder inside the MDAC. When CLK_B is high, MDAC is at sampling phase, V_{SHA} is charged to C_{11} to C_{14}; in the non-overlapping phase between CLK_B and CLK_{BN}, digital outputs from comparators are transferred to the decoder. According to the decoder outputs, one of the voltage references (V_{REFP}, V_{CM} and V_{REFN}) is chosen. When CLK_{AN} turns high, these values are fed to the bottom plate of C_{12}, C_{13} and C_{14} respectively. When CLK_{BN} is high, MDAC is at subtraction and hold phase, charge on C_{12}, C_{13}, C_{14} are transferred to C_{11}, produces the residual output voltage to next stage.

The Default value of capacitors for 1st stage Sub-ADC is C_{11}=C_{12}=C_{13}=C_{14}=0.5pF. Total capacitive loads for SHA are 4pF includes ADC (A) and ADC (B).

The comparator of the 2.5bit MDAC is the 4 inputs full differential comparator. Which used to compare differential input and reference signal, output the compared value. Outputs of six comparators are formed as binary codes, become digital outputs B_{11}, B_{12}, B_{13}. Comparator circuit is shown in Fig. 10.

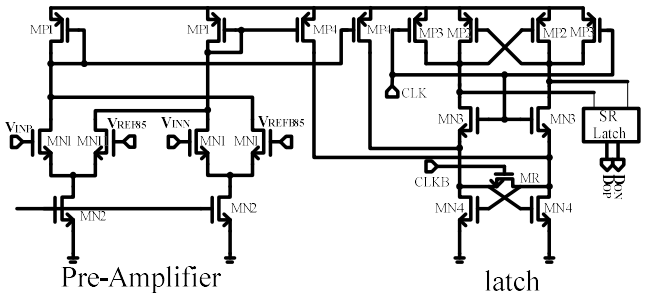


Fig. 10. Comparator circuit.

The comparator composed of pre-amplifier, latch and SR latch circuit. Pre-amplifier is to amplify small difference signal between (V_{INP}-V_{INN}) and (V_{REF85}-V_{REFB85}). Here V_{INP} and V_{INN} are positive and negative held signals from SHA. V_{REF85} and V_{REFB85} is one pair of positive and negative reference signals built by reference buffer. This amplified difference signal is latched when CLK turns high, latch operates as a positive feedback. In this phase, latch generates the output and feeds it to SR latch. When CLKB turns high, comparator works in reset phase. SR latch works as a driver to generate CMOS levels and drives the digital logic gates in the decoder block.

IV. Experimental Results

The proposed split-based pipeline ADC is designed and fabricated in TSMC 0.18um CMOS technology and a nominal supply of 1.8V. The die micrograph of the proposed ADC is shown in Fig. 11. The active area is $3\times4m^2$.

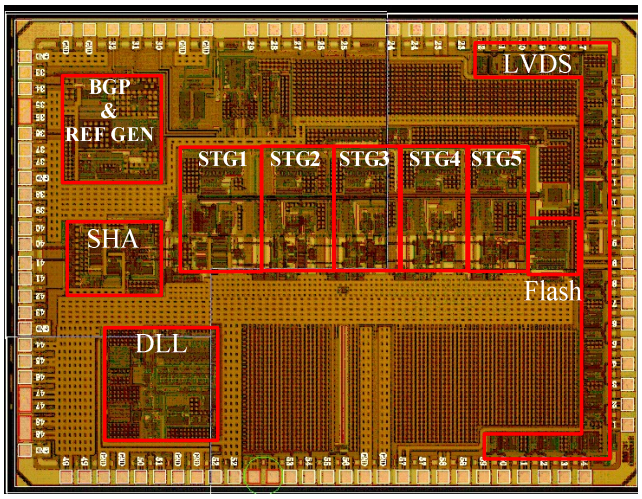


Fig. 11. Micrograph of Proposed ADC.

During chip measurement, the input signal and clock signal are obtained by R&S SMA 100A and Si530 chip respectively. Both were filtered using high order passive band-pass filters around the applied frequency to remove harmonics and white noise produced by signal sources.

Fig. 12 shows the measured static performance of proposed ADC. The ADC differential non-linearity (DNL) and integral non-linearity (INL) are -0.67/+0.62 LSB and -0.79/+0.85 LSB respectively. This performance is obtained without digital calibration technique.

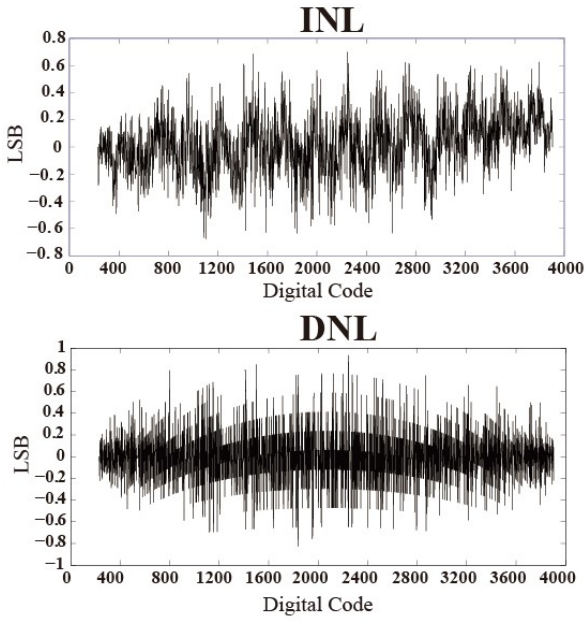
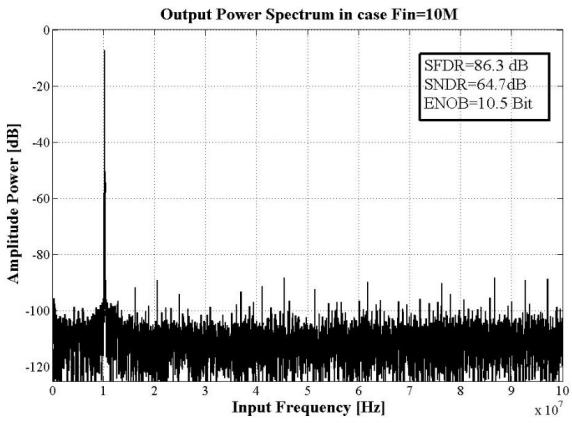
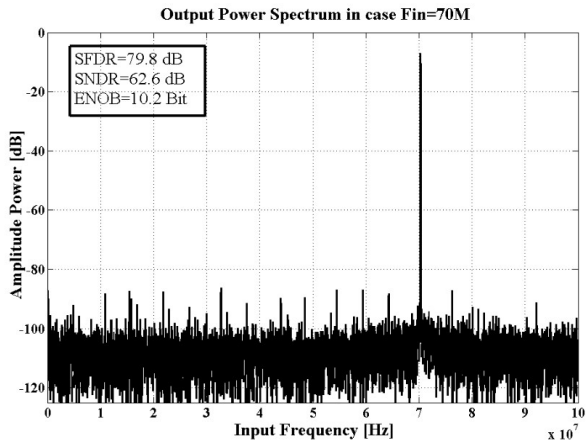


Fig. 12. Measured INL and DNL of proposed ADC.



(a)



(b)

Fig. 13. Output spectrum in case (a) F_{in}=10MHz, (b) F_{in}=70MHz with sampling frequency of 200MHz.

Fig. 13 shows the measured output power spectrum of ADC at sampling frequency of 200MHz and input signal amplitude power of -1dBFS. Fig. 13 (a) gives the dynamic performance of ADC with input signal frequency of 10MHz. Parameters such as SFDR is 86.3dB, SNDR is 64.7dB and ENOB is 10.5 bit are measured. Fig. 13 (b) shows the performance with input signal frequency of 70MHz. Parameters such as SFDR is 79.8dB, SNDR is 62.6dB and ENOB is 10.2 bit are measured. As indicated in Fig. 14, the proposed ADC dynamic performance declines from input signal frequency from 10MHz to 70MHz. the SFDR drops from 86.3dB to 79.8dB. The reason for this decline is the length of bonding wire of the package is more than 2 millimeters, the parasitic inductance of bonding wire decreases the quality of input signal. This parasitic effect becomes serious along with input signal increases. Also the parasitic inductance from bonding wire of power supply induces high frequency noise, which decreases noise dynamic performance of ADC too. This ADC consumes 356mW with power supply of 1.8V. The power distribution of ADC shows in Table III, Table IV summarizes the measured performance of the proposed split-based pipelined ADC and Table V summarizes the performance of this work compares with published papers of pipelined ADCs.

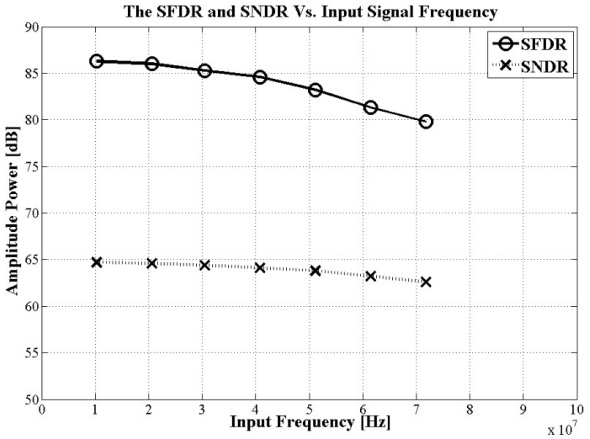


Fig. 14. Measured dynamic performance versus input frequency at 200Msps sampling rate.

TABLE III: THE POWER DISTRIBUTION OF ADC

Circuit component	Power (mW)
SHA	54
Split-based ADC core	120
Band-gap & reference generator	90
DLL	20
Clock Distribution circuit	50
Digital control circuit	22
Power dissipation	356

TABLE IV: MEASUREMENT PERFORMANCE OF PROPOSED ADC

Parameters	Value
Process	0.18um 1P6M CMOS
Power supply	1.8V
Sampling Frequency	200MHz
Input Frequency	10MHz-100MHz
Input signal range	$1.25V_{p-p}$
SNDR @10MHz	64.7 dB
@70MHz	62.6dB
SFDR @10MHz	86.3dB
@70MHz	79.8dB
INL @10MHz	-0.67/+0.62 LSB
DNL @10MHz	-0.79/+0.85 LSB
Clock jitter	$0.5ps_{rms}$
Power dissipation	356mW

TABLE V: PERFORMANCE COMPARISON

	This work	[8]	[9]
Process	0.18um CMOS	90nm CMOS	55nm CMOS
Power supply	1.8V	1.2V	1.1V
Resolution	12bit	12bit	12bit
Sampling rate	200Msps	200Msps	200Msps
SNDR	64.7 dB	64dB	64.6dB
SFDR	86.3dB		82.9dB
INL(LSB)	-0.67/+0.62	-1.70/+1.30	-1.89/+1.36
DNL (LSB)	-0.79/+0.85	-0.59/+0.87	-0.28/+0.24
Power dissipation	356mW	348mW	30.7mW
Digital calibration	Without	With	With

As performance comparison shown in Table V, the proposed split-based ADC has the best SNDR, SFDR performance with low power dissipation without digital calibration.

V. CONCLUSION

This paper describes a split-based 12bit 200Msps pipeline ADC without digital calibration. The proposed ADC distributes sampling capacitances of pipeline ADC into 2 ADC channels, which relaxes requirement of OTA inside each ADC and improves conversion rate of each ADC. The proposed split-based ADC architecture realized high resolution ADC with high conversion rate. Although mismatch between 2 channels reduces the SFDR of ADC, 12 bit resolution can be obtained by careful layout. The chip measurement results confirmed the proposed split-base pipeline ADC achieves SFDR of 86.3dB, SNDR of 64.7dB with input signal frequency of 10MHz and sampling frequency of 200MHz. The power dissipation is 356mW. The proposed split-base pipeline ADC can also be applied to design 4 channels ADC to improve sampling rate speed. It is our future work.

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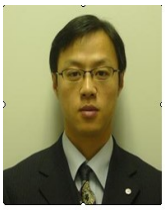

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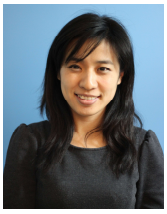

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