High-Speed Designed Area-Efficient Vlsi Architecture Of Three-Operand Binary Adder

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***Abstract*—**The basic functional unit to perform the modular arithmetic in various cryptography and pseudorandom bit generator (PRBG) algorithms is Three-operand binary adder. To perform the three-operand addition Carry-save adder (CS3A) is the widely used technique. However, the ripple-carry stage in the CS3A results in high propagation delay of O(n). To reduce the critical path, delay a parallel prefix twooperand adder such as Han-Carlson (HCA) can be used for three operand addition. But the disadvantages of the architecture are more area and low speed. Hence, a new highspeed and area-efficient adder architecture is proposed using reversible logic. Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backwards or uncomputing the results. This is termed as logical reversibility. The reversible logic design attracting more interest due to its low power consumption. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate.

I. INRTUDUCTION

Most of the pupils of Electronics Engineering are showing to Integrated Circuits (IC's) at a very basic level, involving SSI (small scale integration) circuits like logic gates or MSI (medium scale integration) circuits like multiplexers, parity encoders etc. However, there is vast higher world in the market concerning minimization at levels so satisfactory, that a micrometre and a microsecond are regarded enormous! That is the field of VLSI - Very Large-Scale Integration. The article objectives at seeking to introduce Electronics Engineering scholars to the chances and the work involved in this region. VLSI stands for "Very Large-Scale Integration". That is the area which includes packing increasingly common-sense gadgets into lesser areas. Due to VLSI, circuits that may have taken board full of house can now be put right into a little house few millimetres throughout! This has spread out a large possibility to do matters that were not capable before. VLSI circuits are far and wide. Your pc, your vehicle, your brand-new digital camera, the mobile-telephones, and what have you ever. All this entails numerous advantages on many fronts inside the identical subject, which we will be capable to seem at in later sections. VLSI has been around for an extended time; there may be nothing new about it. However, as a part, outcomes of advances on the planet of computers, there has been a dramatic proliferation of instruments that can be utilized to design VLSI circuits. Alongside, obeying Moore's law, the capability of an IC has increased exponentially over the years, in phrases of computation power, utilisation of to be had discipline, yield. The mixed outcomes of those two advances, is that persons can now put various performance into the IC's, opening new frontiers. Examples are embedded programs, where intelligent instruments are put inside day-to-day objects, and omnipresent computing the place small computing instruments propagate to such an extent that even the footwear you put on may surely do something priceless like monitoring your heartbeats! These two fields are variety an associated, and coming into their explanation can effectively lead to an extra article.

II. REVIEW LITERATURE SURVEY

Block designs and quick functions often employ multi-operand summation (MOS). Research is conducted from a variety of aspects to achieve extremely efficient multioperand addition for medical IoT field devices. Conventional adders used in multipliers and filters for summing of intermediate outputs are prone to area and delay occurrence. There are several adder structures for CLA and PPA that are efficient in terms of delay, but they take up a lot of space and energy, provides a more efficient solution for RCA. As a result, it has been proposed that the carry selection scheme-based adder be used to attain performance comparable to that of the RCA and CLA. It's also one of the quickest adders used in a variety of data-processing

Doi:10.48047/ijiee.2026.16.2.19

applications Carry Select Adder. The CSLA has been extended to reduce the amount of space and power it consumes. Three operand adders and computer systems that support them may be designed using the implementations presented in this thesis. Various application-specific and general-purpose computer architectures may be affected by this. With the ability to affect a wide range of computer systems and engineering and research, this effort has the potential to have a significant impact. To put it another way, the typical general-purpose computer automation (e.g. the Turing machine) is logically irreversible. While keeping their simplicity and capacity to do broad calculations, these machines may be made logically reversible at every step. If thermodynamically reversible computers exist, they may theoretically execute meaningful calculations at practical speeds while using less than KT of energy each logical step. This is significant in the physical sciences. Logically reversible automatons are identical to their non-reversible counterparts, except that they store all intermediate outcomes and avoid the irreversible process of erasure at this stage of computing. The next step is to print out the final product. By retracing the steps of the first stage in reverse order (which is only possible because the first stage was performed reversibly), the third stage then reversibly disposes of all the undesirable intermediate results and returns the machine to its original

III. RESEARCH METHODOLOGY

The proposed work focuses on the design of a high-speed and area-efficient three-operand binary adder suitable for cryptographic and pseudorandom bit generator (PRBG) applications. This section describes the methodology adopted for analyzing existing architectures and developing the proposed reversible logic-based design.

A. Analysis of Existing Architectures

Three-operand addition is commonly implemented using the Carry-Save Adder (CS3A) due to its ability to reduce intermediate carry propagation. However, the final addition stage is typically performed using a ripple-carry adder, resulting in a propagation delay of O(n)O(n)O(n), where nnn is the bit-width.

To overcome this limitation, parallel prefix adders such as the Han–Carlson Adder (HCA) are employed. These architectures reduce carry propagation delay significantly. However, they introduce increased hardware complexity, higher area utilization, and additional interconnect overhead, which limit their efficiency in high-performance and low-power applications.

B. Problem Formulation

From the analysis of existing designs, the following issues are identified:

- High propagation delay in ripple-carry-based CS3A structures
- Increased area and complexity in parallel prefix adders
- Higher power consumption due to irreversible logic operations

These limitations necessitate the development of an alternative architecture that ensures improved speed, reduced area, and lower power dissipation.

C. Proposed Reversible Logic-Based Approach

To address the above challenges, a reversible logic-based three-operand adder architecture is proposed. Reversible computing ensures a one-to-one mapping between input and output vectors, thereby eliminating information loss and reducing energy dissipation.

The proposed design utilizes fundamental reversible gates, including:

- **Feynman Gate** for signal duplication and XOR functionality
- **Fredkin Gate** for controlled data routing and swapping operations

These gates are used to construct reversible half-adder and full-adder modules, which are further extended to support three-operand addition.

D. Design Methodology

The proposed architecture is developed using a hierarchical design approach as follows:

1. Design of reversible half-adder and full-adder circuits
2. Construction of multi-bit reversible adder modules
3. Integration of three-operand addition logic using reversible gate networks
4. Optimization to minimize:
    - Garbage outputs
    - Constant inputs
    - Quantum cost

E. Performance Evaluation Criteria

The performance of the proposed architecture is evaluated and compared with existing CS3A and HCA designs based on the following metrics:

- Propagation delay
- Area complexity
- Power consumption
- Gate count and quantum cost

F. Implementation and Verification

The proposed reversible logic design is implemented using hardware description languages such as Verilog or VHDL. Functional verification is performed through simulation to ensure correct arithmetic operation for all input combinations. The results are analyzed to validate improvements in speed and hardware efficiency.

IV. PROPOSED METHODOLOGY

The proposed methodology presents a reversible logic-based architecture for efficient three-operand binary addition, targeting high-speed and low-power requirements in cryptographic and pseudorandom bit generator (PRBG) applications. The design is developed to overcome the limitations of conventional Carry-Save Adders (CS3A) and parallel prefix adders such as the Han–Carlson Adder (HCA).

A. System Overview

The proposed architecture replaces conventional irreversible adder structures with a reversible logic

Doi:10.48047/ijiee.2026.16.2.19

framework. The system performs three-operand addition using cascaded reversible adder units constructed from fundamental reversible gates. The overall design ensures minimal propagation delay, reduced power dissipation, and optimized hardware utilization.

B. Reversible Logic Design Principle

The proposed method is based on the principle of reversible computation, where each input vector has a unique output vector, ensuring no information loss during processing. This characteristic reduces energy dissipation and is suitable for low-power VLSI design.

The architecture is synthesized using the following reversible gates:

- **Feynman Gate**: Used for signal copying and XOR operations
- **Fredkin Gate**: Used for controlled data routing and multiplexing

These gates form the building blocks for reversible half-adder and full-adder modules.

C. Design of Reversible Adder Unit

The basic reversible full-adder unit is designed by combining Feynman and Fredkin gates to generate sum and carry outputs without producing irreversible data loss. The design is optimized to reduce:

- Garbage outputs
- Constant inputs
- Quantum cost

This reversible full-adder is then extended to multi-bit operations.

D. Three-Operand Addition Architecture

The proposed three-operand addition is implemented by cascading reversible full-adder stages. Unlike CS3A, which relies on a final ripple-carry stage, the proposed design maintains reversibility throughout the computation, thereby eliminating the ripple delay bottleneck.

The architecture processes inputs AAA, BBB, and CCC simultaneously and generates the final sum and carry outputs using a structured reversible logic network.

E. Optimization Strategy

To improve efficiency, the following optimization techniques are applied:

- Reduction of redundant reversible gate usage
- Minimization of garbage outputs through circuit restructuring
- Selection of low quantum cost reversible gate combinations
- Parallel processing of intermediate carry signals

F. Performance Advantages

The proposed methodology provides the following advantages over conventional designs:

- Reduced propagation delay compared to CS3A and HCA
- Lower power consumption due to reversible computation
- Reduced hardware complexity through optimized gate utilization
- Improved suitability for cryptographic hardware applications

V. WORKING PRINCIPLE

The working principle of the proposed reversible logic-based three-operand adder is based on performing arithmetic addition through reversible gate networks while ensuring that no information loss occurs during computation. The architecture operates by transforming input operands into intermediate reversible signals and generating final sum and carry outputs with reduced propagation delay and power dissipation.

A. Input Processing

The system accepts three binary operands AAA, BBB, and CCC of equal bit-width. These inputs are processed simultaneously through reversible logic stages. Each bit position is handled independently using reversible full-adder structures to enable parallel computation across all bit levels.

B. Reversible Logic Operation

The core computation is performed using reversible gates such as the Feynman gate and Fredkin gate. These gates ensure a one-to-one mapping between inputs and outputs, preserving all computational information.

- The **Feynman gate** is used to generate necessary signal copies and perform XOR operations required for sum generation.
- The **Fredkin gate** is used to control data flow and manage conditional carry propagation through reversible switching operations.

C. Sum and Carry Generation

For each bit position, the reversible full-adder unit generates:

- **Sum output (S)** using XOR-based reversible logic operations
- **Carry output (Cout)** using controlled reversible gate configurations

The carry generated at each stage is propagated through optimized reversible paths instead of conventional ripple-carry chains, thereby reducing delay.

D. Three-Operand Addition Process

The three operands are added simultaneously in a structured reversible network. Unlike conventional CS3A, which separates carry-save and final addition stages, the proposed method performs integrated computation using reversible full-adder cascades.

The process can be summarized as:

1. Bitwise reversible addition of inputs AAA, BBB, and CCC
2. Generation of intermediate sum and carry signals
3. Propagation of carry using reversible gate interconnections
4. Final accumulation of sum outputs without information loss

E. Reduction of Delay and Power

The absence of irreversible logic ensures that no bit information is discarded during computation. This reduces

Doi:10.48047/ijiee.2026.16.2.19

heat generation and power dissipation. Additionally, optimized reversible pathways minimize carry propagation delay, improving overall speed compared to ripple-carry-based architectures.
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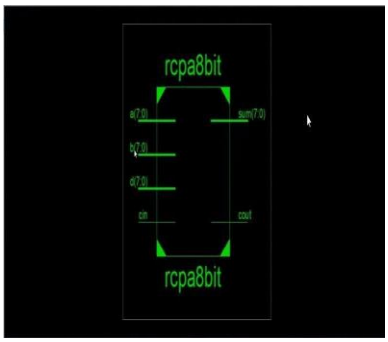
VI. RESULTS AND OUTCOMES

RTL Schematic Output: Once the functional verification is done, the RTL model is taken to the synthesis process using the Xilinx ISE tool. In synthesis process, the RTL model will be converted to the gate level netlist mapped to a specific technology library. The RTL (Register Transfer Logic) can be viewed as black box after synthesizing of design is made. It shows the inputs and outputs of the system. By double-clicking on the diagram, we can see gates, full adder and MUX. Below figure shows the RTL block diagram of implemented design using XILINX-ISE14. From the block diagram we can say implemented design has three inputs a[7:0], b[7:0] and Cin, produces the two outputs sum (7:0)



and

Fig5.1RTLSchematic

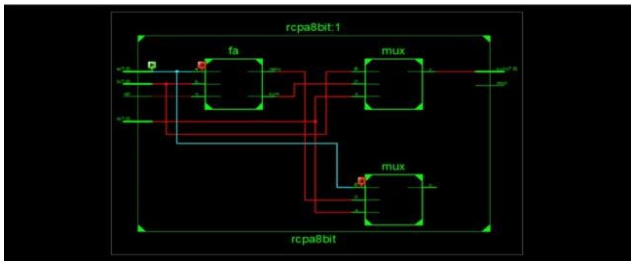


Fig.
Fig5.2:InternalBlockDiagramofRTLSchematic

Fig. 1. FigureshowstheinternalRTLschematicofexistingsystemusingXilinxIse14.Whichis nothing but how the different blocks are connected internally.

Deviceutilizationsummary:

Fig. 2. Thisdeviceutilizationincludesthe following.

- Logic Utilization
- Logic Distribution
- TotalGatecountfortheDesign

Fig. 3. The device utilization summery is shown above in which it gives the details of number of devices used from the available devices and represented in %. Hence as the result of the synthesis process, the device utilization in the used device and package is shown below.

VII. CONCLUSION

The primary objective of this project was to gain insight into the Reversible Computation and its use for making devices energy efficient for long life. To efficiently compute modular arithmetic for use in cryptography and PRBG applications, this study proposes a highspeed, area-efficient adder approach and associated VLSI design. We concludedthatouradderwassuperiortootheraddersby consideringbothareaanddelay.The proposed reversible logic gates reduce the area and propagation delay as it effectively provides negligible loss of information in the circuit. The

Doi:10.48047/ijiee.2026.16.2.19

future scope of this project is, it will be applicable on large amount of data such as 16- bit and 32-bit.

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