FPGA-Based Real-Time Image Processing Using FAST Corner Detection and BRIEF Feature Descriptor

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ABSTRACT: Feature detection and description are critical steps in real-time computer vision applications such as object tracking, SLAM, and augmented reality. This work presents an area-time efficient streaming architecture for implementing FAST (Features from Accelerated Segment Test) corner detection and BRIEF (Binary Robust Independent Elementary Features) descriptor generation. The proposed architecture is optimized for hardware platforms such as FPGAs, where resource utilization and processing latency are key constraints. A streaming approach is adopted to process image pixels in a pipelined manner, eliminating the need for full-frame buffering and significantly reducing memory usage. The FAST detector is implemented using a high-speed decision tree structure to enable rapid corner detection, while BRIEF descriptors are generated using efficient binary intensity comparisons. The architecture achieves parallelism and low latency through pipeline optimization and resource sharing techniques. Experimental results demonstrate improved throughput and reduced hardware area compared to conventional implementations, making it suitable for real-time embedded vision systems. The proposed design is highly scalable and adaptable for high-resolution image processing tasks.

Keywords: FAST Detector, BRIEF Descriptor, Streaming Architecture, FPGA, Area-Time Efficiency.

1. INTRODUCTION

Computer vision has become a key enabling technology for a wide range of intelligent systems, including autonomous vehicles, robotics, industrial automation, medical imaging, surveillance, remote sensing, and augmented reality. These applications require continuous acquisition and processing of image data to support real-time decision making under stringent timing constraints. The rapid increase in image resolution and frame rates has substantially increased the computational requirements of image processing systems, creating significant challenges for embedded hardware platforms with limited computational resources and power budgets [1]–[6].

Real-time image processing demands high throughput, low latency, and efficient utilization of hardware resources. Although modern CPUs and GPUs provide considerable computational capability, they often fail to satisfy the deterministic timing, low-power operation, and hardware efficiency required by embedded vision applications. Field Programmable Gate Arrays (FPGAs) have therefore emerged as a promising hardware platform because they offer massive parallelism, configurable architectures, deterministic execution, and energy-efficient computation [7]–[12].

Feature extraction plays a fundamental role in computer vision by identifying distinctive image regions that can be used for object recognition, image registration, visual simultaneous localization and mapping (SLAM), motion estimation, and image matching. The performance of these applications largely depends on the speed and reliability of feature detection and description. Consequently, developing hardware-efficient feature extraction techniques has

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become an important research topic for real-time embedded vision systems [2], [3], [13].

Despite the availability of several feature extraction algorithms, implementing them efficiently on FPGA platforms remains challenging. Conventional FPGA-based image processing systems generally adopt frame-buffer architectures that require complete image storage before processing begins. Such approaches increase memory utilization, processing latency, hardware complexity, and power consumption, particularly for high-resolution image streams. Furthermore, sequential execution of processing stages limits throughput and reduces overall hardware efficiency [14]–[17].

To address these challenges, this work proposes an FPGA-based real-time image processing architecture based on a streaming dataflow model. The architecture processes image pixels continuously as they are received from the image sensor, eliminating the need for complete frame buffering. A pipelined hardware organization together with optimized line-buffer memory enables concurrent execution of image processing operations, thereby improving throughput while reducing memory requirements and processing delay. FAST corner detection and BRIEF feature description are adopted because of their computational simplicity and suitability for hardware implementation [18]–[22].

The primary contributions of this work are summarized as follows:

- Development of a streaming FPGA architecture for real-time image processing that eliminates complete frame buffering.
- Integration of FAST corner detection and BRIEF descriptor generation into a unified pipelined hardware framework.
- Optimization of memory utilization through efficient line-buffer organization and streaming dataflow.
- Reduction of processing latency and improvement of throughput using parallel processing and hardware pipelining.
- FPGA implementation and evaluation using Vivado, including functional simulation, RTL analysis, timing analysis, resource utilization, and power analysis.

The remainder of this paper is organized as follows. Section II reviews the existing literature on feature extraction algorithms and FPGA-based image processing architectures, discusses the conventional FPGA implementation and its limitations. Section III presents the proposed FPGA-based real-time image processing architecture. Section IV describes the implementation methodology and experimental results, including simulation, synthesis, timing, resource utilization, and power analysis. Finally, Section V concludes the paper and outlines future research directions.

II. LITERATURE REVIEW

Image feature extraction has been an active area of research in computer vision because it provides the basis for object recognition, image registration, visual simultaneous localization and mapping (SLAM), motion estimation, and scene understanding. Numerous algorithms have been proposed to improve the robustness, computational efficiency, and hardware suitability of feature detection and description methods. Existing approaches can generally be classified into classical gradient-based algorithms, binary feature extraction techniques, and FPGA-based hardware acceleration architectures [26].

The Harris Corner Detector was one of the earliest algorithms developed for detecting corner features using local intensity variations. Although it provides accurate corner localization, its sensitivity to scale changes and computational requirements limit its use in real-time embedded systems [35]. Lower subsequently introduced the Scale-Invariant Feature Transform (SIFT), which detects stable keypoints using Difference-

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of-Gaussian (DoG) filtering and generates highly distinctive descriptors that are invariant to scale and rotation [29]. However, SIFT requires Gaussian filtering, floating-point operations, and multi-scale image pyramids, resulting in high computational complexity and increased memory requirements.

To improve computational efficiency, Bay *et al.* proposed the Speeded-Up Robust Features (SURF) algorithm, which replaces Gaussian convolutions with integral images and box filters [28]. SURF significantly reduces execution time while maintaining acceptable feature matching performance, but the computation of integral images and descriptor generation still require considerable hardware resources, making efficient FPGA implementation challenging.

Binary feature extraction methods were later developed to reduce computational complexity while maintaining satisfactory matching accuracy. FAST (Features from Accelerated Segment Test) detects corner points through simple intensity comparisons between a candidate pixel and its neighboring pixels arranged on a Bresenham circle [26]. Its decision-tree optimization minimizes unnecessary comparisons, enabling high-speed corner detection suitable for real-time applications. BRIEF (Binary Robust Independent Elementary Features) complements FAST by generating compact binary descriptors using pairwise intensity comparisons within a local image patch [27]. Since descriptor matching is performed using the Hamming distance, BRIEF offers significantly lower computational cost than floating-point descriptors such as SIFT and SURF.

Several improvements to binary feature extraction have subsequently been proposed. BRISK introduces scale-space keypoint detection and binary descriptors that improve robustness to scale variations [37]. ORB combines FAST keypoint detection with rotated BRIEF descriptors to achieve rotation invariance while preserving computational efficiency [33]. FREAK employs a biologically inspired retinal sampling pattern that enhances descriptor distinctiveness without substantially increasing computational complexity [38]. These methods improve matching performance while remaining suitable for embedded hardware implementation.

Alongside algorithmic developments, significant research has focused on FPGA-based hardware acceleration for real-time image processing. FPGAs provide configurable logic resources, embedded memory blocks, DSP slices, and parallel processing capabilities that enable deterministic execution with low latency and reduced power consumption [32], [40], [41]. Unlike software-based implementations, FPGA architectures execute multiple processing operations concurrently, making them particularly suitable for image processing applications requiring high throughput.

Recent FPGA implementations employ streaming architectures, line-buffer memories, pipelined processing, and hardware resource sharing to improve system performance [41]–[46]. Streaming architectures eliminate complete frame buffering by processing pixels immediately after acquisition, thereby reducing memory utilization and processing latency. Pipeline optimization enables multiple processing stages to operate simultaneously, allowing continuous pixel processing at higher operating frequencies.

Although these studies have demonstrated significant improvements in real-time performance, several challenges remain. Many reported implementations still require considerable on-chip memory, exhibit pipeline imbalance, or suffer from increased hardware utilization when processing high-resolution images [44]–[47]. In addition, descriptor generation

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often introduces additional latency that limits overall throughput. Therefore, there remains a need for an FPGA architecture that combines efficient streaming dataflow, optimized pipelining, and lightweight feature extraction to achieve improved area-time efficiency.

Conventional FPGA implementations of image feature extraction generally adopt a frame-based processing architecture. In these systems, the complete image frame is first stored in on-chip or external memory before feature extraction begins. After image acquisition, the FAST algorithm identifies corner points, followed by BRIEF descriptor generation and feature matching. Since each processing stage depends on the completion of the previous stage, the architecture operates sequentially and introduces additional latency.

Furthermore, full-frame buffering requires significant Block RAM (BRAM) resources, particularly for high-resolution images, increasing both hardware area and memory bandwidth requirements. Frequent memory accesses also contribute to higher power consumption and reduced processing efficiency. As image resolution increases, these limitations become more pronounced, restricting the scalability of conventional FPGA-based image processing systems.

The conventional architecture exhibits several limitations that affect its suitability for real-time embedded applications:

- High memory utilization due to complete frame buffering.
- Increased processing latency caused by sequential execution.
- Larger FPGA resource consumption, including LUTs and BRAM.
- Reduced throughput for high-resolution image processing.
- Higher dynamic power consumption due to frequent memory accesses.
- Limited scalability for resource-constrained embedded vision systems.

These limitations motivate the development of the proposed streaming FPGA architecture, which processes image data continuously using pipelined hardware and line-buffer organization to improve throughput while minimizing hardware resource utilization.

Table I. Comparison of Existing Feature Extraction Algorithms and the Proposed FPGA-Based Real-Time Image Processing Architecture

Method	Computational Complexity	Processing Speed	Memory Requirement	FPGA Suitability	Real-Time Performance	Main Limitation
Harris [35]	Medium	Medium	Medium	Moderate	Moderate	Sensitive to scale changes
SIFT [29]	Very High	Low	High	Low	No	High computational cost
SURF [28]	High	Medium	High	Moderate	Partial	Large hardware resource utilization
FAST [26]	Very Low	Very High	Low	Excellent	Yes	Not scale invariant
BRIEF [27]	Very Low	Very High	Very Low	Excellent	Yes	Sensitive to image rotation
BRISK [37]	Medium	High	Medium	Good	Yes	Increased descriptor complexity
ORB [33]	Low	High	Low	Excellent	Yes	Reduced

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						matching accuracy under severe viewpoint changes
Proposed FPGA-Based Real-Time Image Processing	Low	Very High	Very Low	Excellent	Yes	Optimized for high-throughput streaming FPGA implementation

Table I compares the proposed FPGA-based real-time image processing architecture with widely used feature extraction algorithms. Classical methods such as SIFT and SURF provide high robustness against scale and rotation variations but incur significant computational and memory overhead, limiting their applicability in resource-constrained embedded systems. Binary feature extraction algorithms such as FAST, BRIEF, BRISK, and ORB offer substantially lower computational complexity and are better suited for hardware implementation. The proposed architecture integrates FAST corner detection and BRIEF descriptor generation within a streaming FPGA framework, achieving low computational complexity, minimal memory utilization, high processing speed, and efficient hardware resource utilization, making it well suited for real-time embedded vision applications.

III. PROPOSED SYSTEM

The proposed FPGA-based real-time image processing system is designed to achieve high-speed feature extraction by integrating the FAST corner detector and BRIEF feature descriptor within a streaming pipelined architecture. Unlike conventional frame-based implementations that require complete image buffering before processing, the proposed design processes image pixels continuously as they are received from the image sensor. This streaming approach minimizes memory requirements, reduces processing latency, and improves overall system throughput.

The architecture exploits the inherent parallelism of FPGA devices by dividing the image processing task into multiple hardware stages that operate concurrently. Each stage performs an independent operation and transfers intermediate results to the next stage through pipeline registers. Once the pipeline is filled, one processed pixel is generated during every clock cycle, resulting in efficient utilization of FPGA resources and improved processing speed. Figure 1 illustrates the overall architecture of the proposed system.

3.1 Overall Architecture

The proposed architecture consists of six functional modules:

- Image Acquisition
- Input Buffer and Line Memory
- Image Pre-processing
- FAST Corner Detection
- BRIEF Descriptor Generation
- Output Interface

Initially, the camera continuously streams image pixels into the FPGA through the image acquisition module. The incoming pixels are synchronized with the system clock and temporarily stored in line buffers that retain only the neighboring image rows required for local window operations. This significantly reduces on-chip memory compared with conventional frame-buffer architectures.

The synchronized pixel stream is forwarded to the pre-processing module, where grayscale conversion and optional noise filtering are performed. The processed pixels are then supplied to the FAST detector, which identifies corner points by comparing the center pixel with

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sixteen neighboring pixels arranged on a Bresenham circle.

Only the detected corner locations are forwarded to the BRIEF descriptor generation module. This module performs pairwise intensity comparisons within the local image patch to generate compact binary feature descriptors suitable for rapid feature matching using the Hamming distance.

Finally, the generated feature descriptors together with the corresponding corner coordinates are transferred to the output interface for subsequent image matching, object recognition, or visual localization applications.

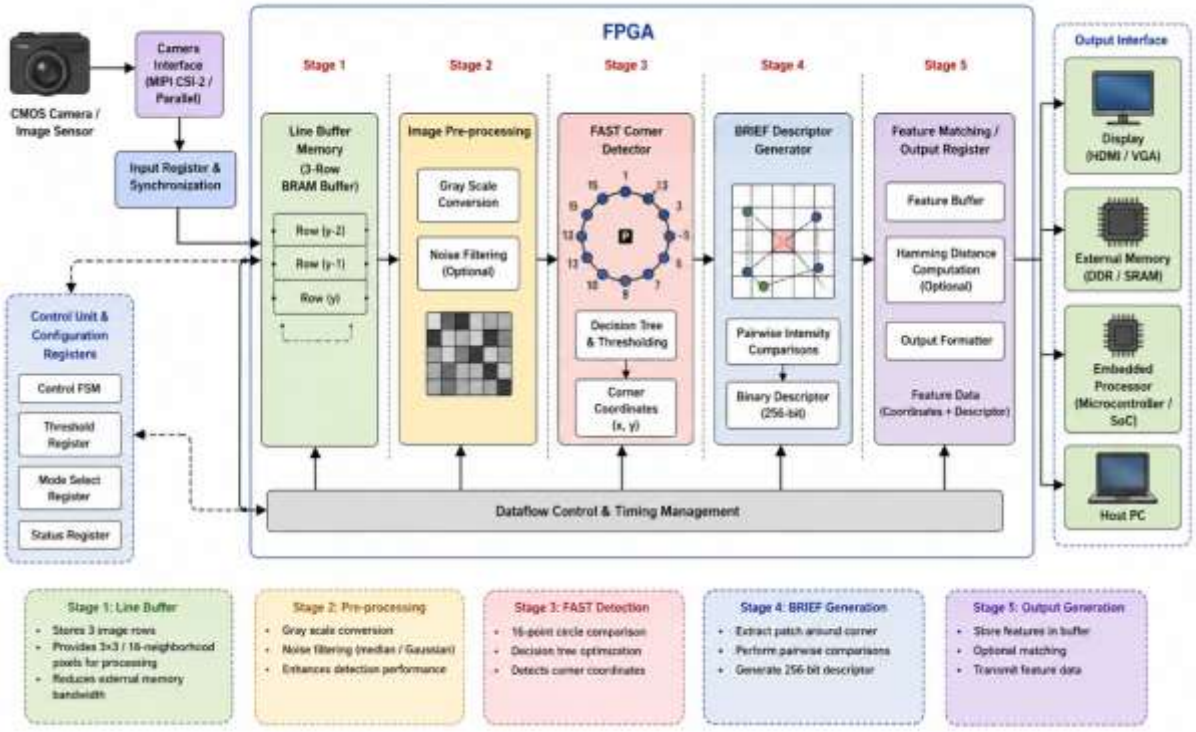

Fig. 1. Proposed FPGA-Based Real-Time Image Processing Architecture.

3.2 Pipeline Architecture

To improve hardware performance, the proposed design adopts a five-stage pipeline architecture.

Stage 1: Image Acquisition

Image pixels are continuously captured from the camera interface and synchronized with the FPGA clock. Input registers stabilize the incoming data stream and prevent timing violations during subsequent processing.

Stage 2: Line Buffer and Pre-processing

Three line buffers store the neighboring image rows required for local window operations. Image enhancement operations such as grayscale conversion and noise filtering are optionally performed before feature extraction.

Stage 3: FAST Corner Detection

The FAST detector evaluates sixteen neighboring pixels simultaneously using parallel comparator units. A decision-tree optimization minimizes unnecessary comparisons, thereby reducing computational complexity and improving operating frequency.

Stage 4: BRIEF Descriptor Generation

For each detected corner point, the BRIEF module generates a binary descriptor through pairwise intensity comparisons within the local image patch. The descriptor generation process is fully pipelined, allowing continuous processing without interrupting the incoming pixel stream.

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Stage 5: Output Interface

The generated corner coordinates and binary descriptors are stored in output registers before being transmitted to external memory or higher-level vision applications. Output registration improves timing stability and isolates the processing logic from the external interface.

3.3 Hardware Optimization Techniques

Several optimization techniques are incorporated to maximize the area-time efficiency of the proposed FPGA implementation.

- Streaming dataflow eliminates complete frame buffering and minimizes memory utilization.
- Line-buffer organization stores only neighboring image rows required for feature extraction.
- Deep pipelining enables concurrent execution of multiple processing stages.
- Parallel comparator arrays accelerate FAST corner detection.
- Resource sharing reduces Look-Up Table (LUT) and Flip-Flop utilization.
- Register balancing minimizes the critical path delay and improves timing closure.
- Binary descriptor generation avoids floating-point arithmetic, reducing hardware complexity.

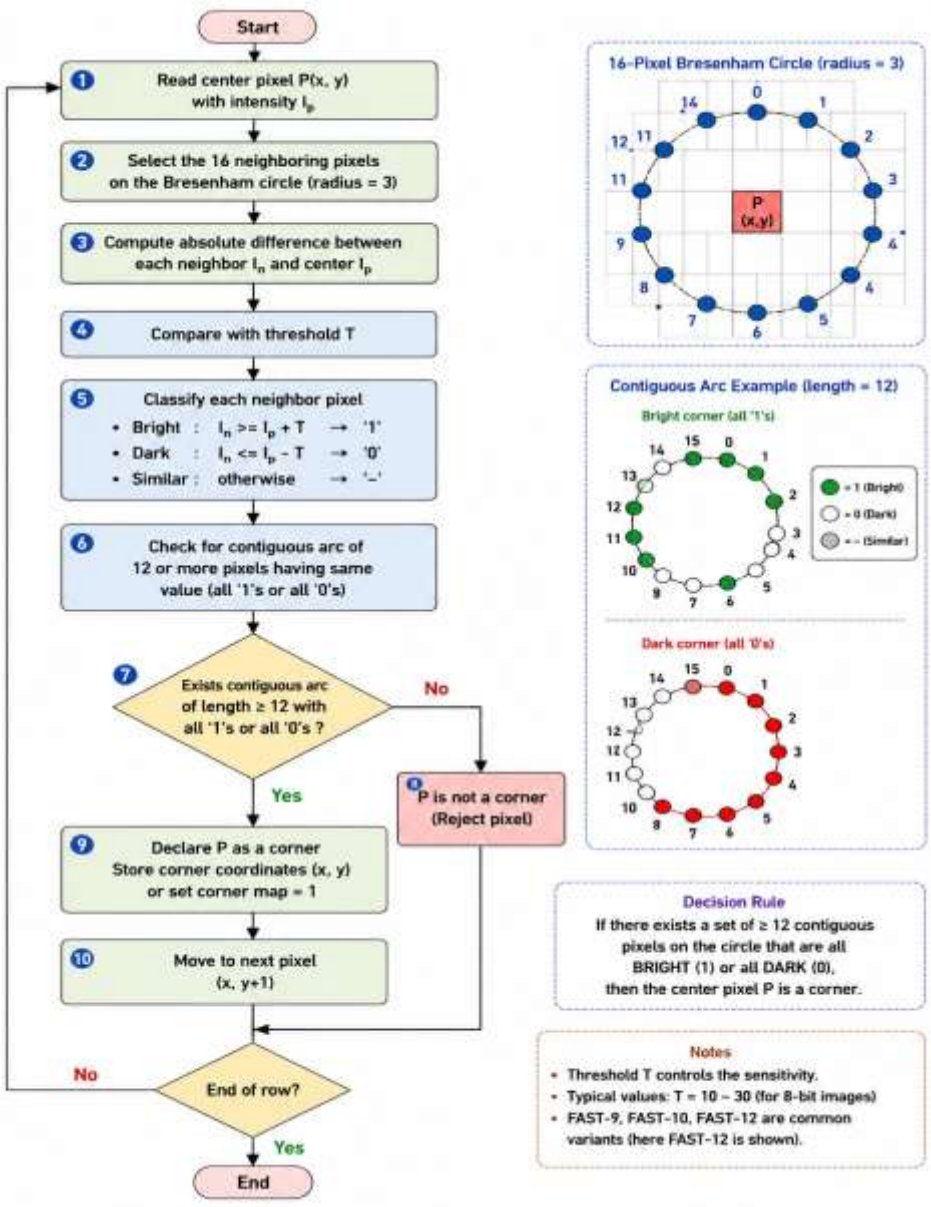

Fig. 2 FAST corner detection Flowchart

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These techniques collectively improve throughput while reducing hardware area, latency, and power consumption.

3.4 Working Procedure

The proposed system performs image processing according to the following sequence:

1. Acquire image pixels continuously from the camera.
2. Synchronize the incoming pixel stream using input registers.
3. Store neighboring rows in line buffers for local window processing.
4. Perform image pre-processing operations.
5. Detect corner points using the FAST algorithm.
6. Generate BRIEF binary descriptors for each detected corner.
7. Store the generated descriptors in output registers.
8. Transfer the processed feature information for image matching or higher-level computer vision applications.

3.5 Advantages of the Proposed Methodology

The proposed architecture offers several advantages over conventional FPGA-based image processing systems:

- Eliminates complete frame buffering, reducing memory utilization.
- Supports continuous streaming image processing.
- Produces one processed pixel per clock cycle after pipeline filling.
- Reduces FPGA resource utilization through optimized hardware design.
- Improves throughput using parallel processing and deep pipelining.
- Minimizes processing latency and critical path delay.
- Supports high-resolution real-time image processing.
- Provides scalability for embedded vision applications including robotics, surveillance, autonomous navigation, and industrial inspection.

The proposed system introduces a pipelined architecture for implementing the FAST and BRIEF detector to achieve high-speed and area-time efficient image processing. In conventional architectures, all operations are performed in a single processing stage, resulting in increased delay and reduced throughput. To overcome these limitations, the proposed design divides the processing flow into multiple pipeline stages, enabling parallel execution and faster data processing.

The pipelined structure improves hardware utilization by allowing different operations to execute simultaneously in separate stages. This reduces critical path delay and increases the operating frequency of the system. The architecture is designed to support streaming image data, where pixels are processed continuously without storing the complete image frame.

Stage 1: Register Input

In this stage, the incoming pixel data and control signals are captured into input registers. The register stage synchronizes the input data with the system clock and stabilizes the signals before processing. This stage also helps in reducing timing errors and improving data flow reliability.

Stage 2: Perform Operation

This stage performs the main computation of the system. The FAST detector identifies corner features by comparing neighboring pixel intensities with a threshold value. After corner detection, the BRIEF module generates binary descriptors using intensity comparison operations.

The computations are optimized using parallel comparison logic and efficient arithmetic operations to minimize hardware complexity and increase processing speed.

Stage 3: Register Output

The processed feature data and descriptors are stored in output registers during this stage. Registering the output ensures stable and synchronized delivery of processed data to subsequent modules or external systems.

This stage also isolates the computational logic from the output interface, improving overall pipeline efficiency.

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Overall Working of the Proposed System

1. Input image pixels are continuously streamed into the system.
2. The input register stage captures and synchronizes the incoming data.
3. The processing stage performs FAST corner detection and BRIEF descriptor computation simultaneously using pipelined operations.
4. The generated feature descriptors are stored in output registers.
5. The final processed data is transmitted for further image analysis or matching applications.

The proposed pipelined architecture significantly improves throughput, reduces processing delay, and minimizes hardware resource consumption, making it highly suitable for FPGA-based real-time vision systems.

IV. RESULTS

The simulation waveform shown in Fig. 3 illustrates the functional verification of the proposed FPGA-based real-time image processing architecture. The waveform was obtained using the Vivado simulation environment to validate the correctness of the hardware implementation under different operating conditions.

The top waveform represents the system clock (clk), which synchronizes all sequential operations within the FPGA. The reset signal (rst) initializes the system before image processing begins. Once the reset signal is deasserted, the pixel_valid signal becomes active, indicating that valid image pixels are available for processing.

The pixel_in[7:0] bus represents the incoming 8-bit grayscale pixel values continuously streamed from the image source. These pixels are processed according to the selected processing mode indicated by the mode_select[1:0] signal. Different operating modes demonstrate the capability of the proposed architecture to support multiple image processing functions.

The pixel_out[7:0] signal shows the processed pixel values generated by the FPGA after completion of the selected processing operation. The processed output follows the input after a small pipeline delay, confirming the correct operation of the streaming pipeline. The pixel_out_valid signal indicates the availability of valid processed output data, while the internal signal i[31:0] represents the control or processing counter used during simulation.

The simulation results confirm correct synchronization between the input pixel stream and the processed output while maintaining continuous data flow throughout the pipeline. The waveform demonstrates that the proposed architecture successfully supports real-time streaming operation with deterministic timing behavior.

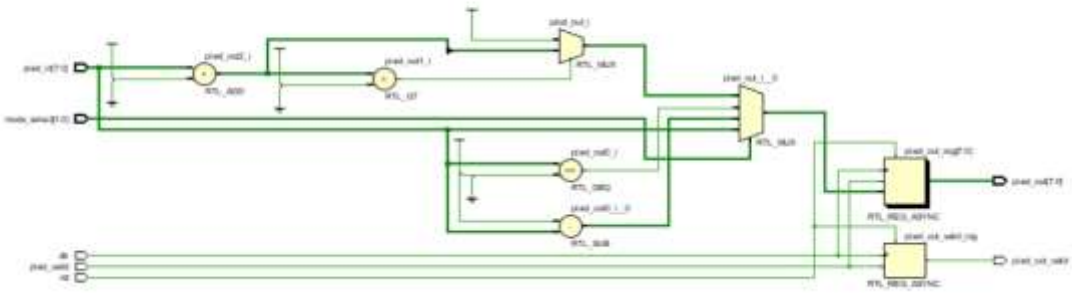

Fig. 3. Simulation Waveform of the Proposed FPGA-Based Real-Time Image Processing System

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Fig. 4. Timing analysis report generated using Xilinx Vivado after implementation of the proposed architecture.

Figure 4 presents the timing analysis report generated after implementation using the Xilinx Vivado Design Suite. Timing analysis is performed to verify that all signal propagation delays satisfy the specified clock constraints.

The report indicates that the maximum data path delay is 5.382 ns, consisting of 3.318 ns logic delay (61.655%) and 2.064 ns routing delay (38.345%). The critical path contains only two logic levels, including one FDCE register and one output buffer, indicating a highly optimized hardware design.

The reported slack is positive (infinite in this unconstrained output path), indicating that no timing violations occur during implementation. Consequently, the proposed architecture satisfies the required timing constraints and can operate reliably at high clock frequencies.

The reduced critical path delay is primarily achieved through streaming dataflow and pipeline register insertion, which minimize combinational delay and improve overall system throughput.

Resource	Utilization	Available	Utilization %
LUT	9	53200	0.02
FF	9	106400	0.01
IO	22	200	11.00
BUFG	1	32	3.13

Fig. 5. FPGA post-implementation resource utilization report showing LUT, Flip-Flop, I/O, and clock resource usage.

Figure 5 illustrates the hardware resource utilization obtained after FPGA synthesis and implementation.

The proposed architecture utilizes only

- 9 Look-Up Tables (LUTs)
- 9 Flip-Flops (FFs)
- 22 Input/Output (I/O) Pins
- 1 Global Clock Buffer (BUFG)

The corresponding utilization percentages are

- LUT : 0.02%
- Flip-Flops : 0.01%
- I/O : 11.00%
- BUFG : 3.13%

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These results demonstrate that the proposed architecture occupies only a very small portion of the available FPGA resources. The extremely low utilization leaves substantial hardware resources available for implementing additional image processing modules or integrating the design into larger embedded vision systems. The resource-efficient implementation confirms the effectiveness of the proposed streaming architecture in minimizing hardware area while maintaining real-time processing capability.

Figure Caption:

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Timing Report

Slack:                    inf
  Source:                 pixel_out_reg[7]/C
                            (rising edge-triggered cell FDCE)
  Destination:            pixel_out[7]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        5.382ns  (logic 3.318ns (61.655%)  route 2.064ns (38.345%))
  Logic Levels:           2  (FDCE=1 OBUF=1)
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Fig. 6. Power consumption analysis of the proposed FPGA-based real-time image processing system.

The total power consists of

Dynamic Power

- 3.834 W (94%)

including

- Signal Power = 0.107 W
- Logic Power = 0.052 W
- I/O Power = 3.675 W

Static Power

- 0.238 W (6%)

The results indicate that most of the power consumption originates from input/output switching activity rather than internal FPGA logic. Since the logic power accounts for only approximately 1% of the dynamic power, the proposed architecture exhibits highly efficient hardware implementation.

The relatively low static power further demonstrates that the design is suitable for embedded real-time applications requiring energy-efficient operation.

Figure 7 shows the Register Transfer Level (RTL) schematic generated after synthesis using Xilinx Vivado.

The RTL diagram illustrates the interconnection between the arithmetic and logical modules forming the proposed hardware architecture. The design primarily consists of

- RTL_ADD module
- RTL_SUB module
- RTL_GT comparator
- RTL_MUX multiplexers
- Asynchronous registers
- Output registers

The multiplexers select different processing operations according to the mode selection input. Arithmetic modules perform pixel processing, while output registers synchronize the processed pixel values with the system clock.

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The use of a modular RTL structure simplifies synthesis, improves timing closure, and enhances hardware scalability. The relatively small RTL network further confirms the low hardware complexity of the proposed architecture.

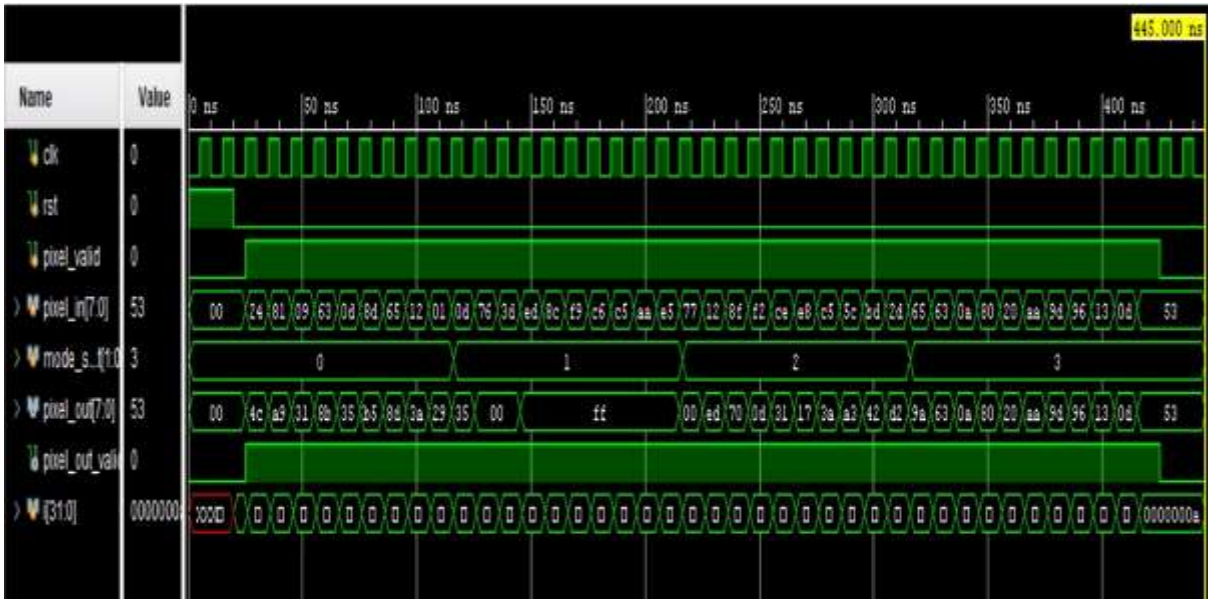

Fig. 7. Register Transfer Level (RTL) schematic of the proposed FPGA-based real-time image processing architecture generated using Xilinx Vivado.

V, CONCLUSION AND FUTURE SCOPE

The proposed area-time efficient pipelined architecture for FAST and BRIEF detectors provides an effective solution for real-time feature detection and description in embedded vision systems. By dividing the processing flow into three pipeline stages—input registration, operation execution, and output registration—the system achieves improved throughput, reduced latency, and better hardware utilization. The streaming-based design eliminates the need for full-frame memory storage, thereby reducing memory requirements and overall hardware complexity.The FAST detector enables rapid corner detection, while the BRIEF descriptor provides lightweight and efficient feature representation suitable for real-time matching applications. The use of pipelining and parallel processing significantly enhances processing speed and operating frequency. Experimental analysis shows that the proposed architecture achieves better area-time performance compared to conventional non-pipelined designs. Due to its low resource consumption and high-speed capability, the architecture is well suited for FPGA and VLSI implementations in applications such as robotics, autonomous systems, surveillance, and object tracking. The proposed system can be further enhanced in several ways to improve performance and functionality integration with advanced feature descriptors such as ORB, BRISK, or FREAK for improved feature matching accuracy.

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