Design of Master Data Acquisition Module for Data Acquisition and Telemetry Operations

C. H. Sanjay, Satyanarayana Kumari B., and Kasetty Ram Babu

***Abstract*—The paper describes Design of Master Data Acquisition module which is used for analog data acquisition from various sensors in satellite subsystems and also performs generation of different telecommands for telemetry operation. Data Acquisition plays an important role in monitoring the health parameters of the satellite. The embedded software was designed to receive input from various sensors and downlinked to the Command and Data Acquisition (CDA) Station and sent to the Satellite Operations Control Center (SOCC) and initiate corrective action form earth control station when required. This methodology was not compromised with respect to the application and execution time. The advent of Field Programmable Gate Arrays (FPGAs) has made compact realization of embedded system possible. As FPGAs are high density logic devices. It is possible to realize certain software functions in hardware in an efficient way. In this paper it is an approach of designing Data Acquisition in Hardware, an input multiplexer is used to route data from various sensors. The selection of channel in the multiplexer, generation of control signal and data reading is performed by Master Data Acquisition module. Entire Design is carried out usingVery High Speed Integrated circuit (VHSIC) Hardware Description Language.**

***Index Terms*—Data acquisition, data converters, telemetry, bus management unit.**

I. Introduction

The satellite control system in general is designed to monitor the various health parameters of the satellite and initiate corrective actions whenever required [1]. The control system receives data from various monitoring sensors and beams them down to the earth control station for processing. Many standalone electrical systems can be integrated into a single system with advances in spacecraft technologies resulting in miniaturization in spacecraft electronics. Hence the design of spacecraft electronics is governed by overriding concern to reduce power, weight and volume. With high speed processors, Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs), several subsystems are integrated into a single Bus Management Unit (BMU).

Several stand-alone systems like Master Data Acquisition system, On-board storage and playback logic, Timer control, Sensor electronics, Temperature controller, 1553 bus protocol, Attitude and Orbit Control Electronics (AOCE) and Telemetry (TM) are integrated into a single BMU. Bus management system is a centralized information processing system. Thus, the design of the BMU is governed by compact realization at package level, minimal interfaces at spacecraft level and operational consideration at mission level [1].

BMU does command, monitoring, data acquisition functions in addition to Attitude and Orbit Control functions.

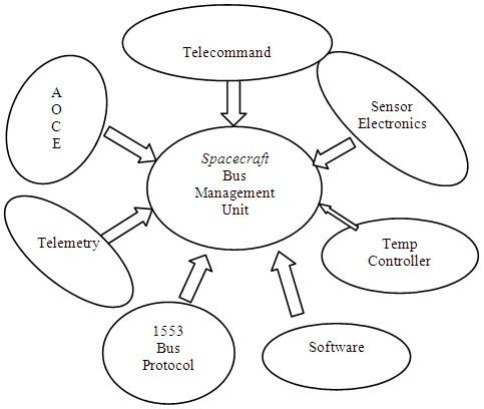

Fig. 1. Integration of stand-alone sub-system into spacecraft BMU.

The Master Data Acquisition (MDA) is the module integrated in the BMU which is mainly utilized for analog data acquisition from various sensors in satellite subsystems and also performs generation of different telecommands for telemetry operation. This MDA can be easily implemented using Hardware Description Language.

The note is organized as follows: Section 2 describes Bus Management System; Section 3 describes the Master Data Acquisition and its details; Section 4 gives the implementation of analog data acquisition using VHDL with Modelsim simulation results.

II. Bus Management Unit

A. Motherboard Configuration

BMU is realized as a Mother-board Daughter-board package. A standard bus is present on the Mother board of BMU to simplify the design of daughter boards and to have flexibility of slot independency. A few new technologies introduced are Bus Management Unit for carrying out functions such as Command, Telemetry, Attitude and Orbit Control, Sensor Processing [1]. A common bus is used for all the Daughter cards, which is routed through the motherboard. This is done to simplify the design of the daughter cards.

B. Daughter Card Configuration

Signals from other systems of the spacecraft are routed to

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the appropriate Daughter card directly. The Daughter card is housed in a tray. The design of the tray is such that the PCB is not exposed to the external world to minimize effects of EMI/radiation. It also allows double side mounting of components. The design of the tray is standardized to simplify the fabrication process. Fig. 2 shows the Motherboard-Daughter-board configuration. On the spacecraft deck, one side of the tray is flush mounted, as it leads to better thermal conduction.

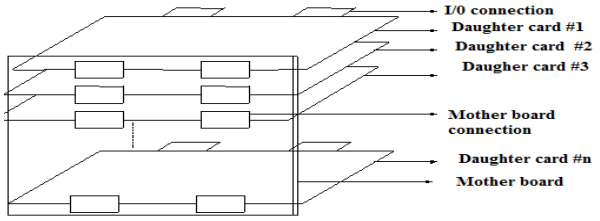

Fig. 2. Mother board-daughter board configuration.

III. Master Data Acquisition

The Master Data Acquisition module is used for analog data acquisition from various sensors in satellite subsystems and also performs generation of different telecommands for telemetry operations. The Interface of MDA Module along with subsystems is shown in Fig. 3 below.

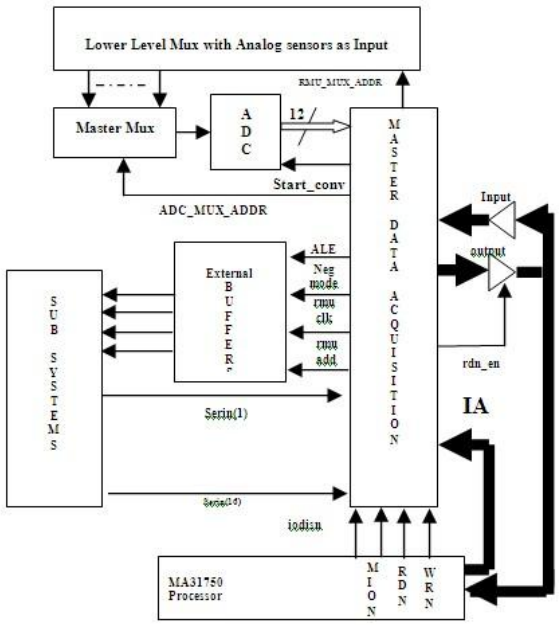

Fig. 3. Interface of MDA module with other subsystems.

The MDA module houses a group of functional blocks for various operations such as analog data acquisition, Remote Multiplexer Unit (RMU) interface, Digital telemetry, Normal and Dwell telemetry, On-board timer (OBT), and other event time latching and monitoring, Status monitoring like Solar panel deployment, major and minor cycle flags, and different clock generation. It also generates different telecommand for telemetry operations [3].

The Functional blocks in MDA are IO Interface, Analog Strobe Generation, Remote Multiplexer Unit (RMU) Interface, Deployment and Command status, Telemetry for Digital Words, Minor Cycle Flag Generation, Clock and Mode Generation, Telecommand Generation, Normal Telemetry, Dwell/Playback Telemetry, OBT Counter and OBT Latch. The Block Diagram of MDA is shown in Fig. 4 below.

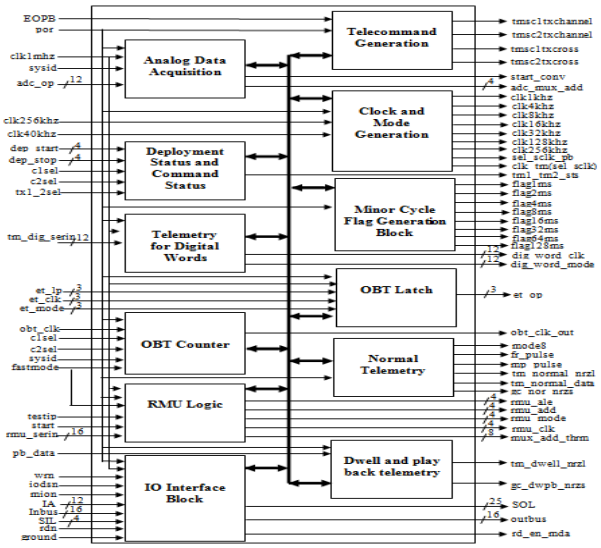

Fig. 4. Block diagram of master data acquisition.

A. IO Interface

This block is used to write or read data in appropriate register such as normal data, dwell data, telecommands data for both link1 and link2, RMU Multiplexer Address, OBT by the processor, The IO interface block is provided. This basically has 12-bit address lines from processor Input Address (11:0), control lines such as write, read and input and output port address [3].

B. Analog Data Acquisition

This block is used to for analog data acquisition form different sensors form satellite subsystems. The muxed output is sent to Analog to Digital Converter (ADC) and with the start of conversion signal the analog data in converted to digital data. The converted data which is of 12-bit data from ADC is the latched and sent to the processor for further processing. The block diagram of the analog acquisition is shown below in Fig. 5 Analog acquisition is performed when indicated by the start of conversion pulse [3].

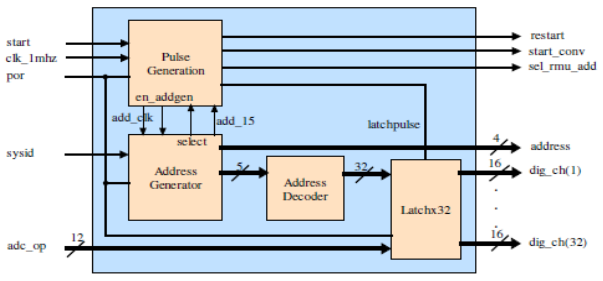

Fig. 5. Analog data acquisition.

The pulse generation logic generates pulse such as start of conversion pulse and then latching the data to different sets of latches during normal and dwell acquisition. The address generator generates the address for normal and dwell latches at suitable time instant that are decoded by the address decoder. The pulse generation logic generates the pulses

specified in the timing diagram.

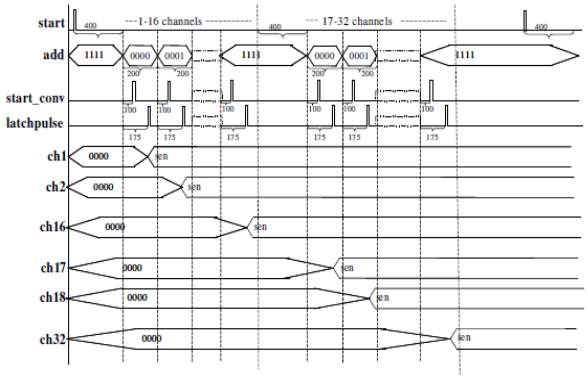

Fig. 6. Timing specifications for analog data acquisition.

C. Remote Multiplexer Unit Logic

The block has interface with 16 RMUs. The Interface is provided to send serial address (8-bit), mode, clock, address latch enable (ALE), to acquire the data from other RMU. Two IO latches are provided for the normal and dwell RMU address, the upper 8-bits are send to the thermal sensors of the satellite whereas the lower 8-bits send serially as address to the subsystem. Address switch occurs when there is transition from normal to dwell data acquisition. Provision is made so that RMU data is latched four times to the latches before read by the processor to mitigate the asynchronisms and complete ensure data latching. The latched 8-bit data output are combined to make 16-bit word, which is read by the processor. Two consecutive serial lines are (odd number is mapped as LSB word, even is mapped as MSB word) mapped to a 16-bit word in which the LSB 8 bits are mapped to the odd number channel whereas the upper 8 MSB bits are mapped to even number channels. However, in contrary to this notation, the 8 bits digital telemetry words are mapped in opposite order (odd number is mapped as MSB word, even is mapped as LSB word) and software should appropriately map them as needed.

D. Telemetry for Digital Words.

Telemetry of digital words from different subsystems is realized using this block. Twelve serial channels are monitored by the processor. This provides the functional interface between the spacecraft and ground command and control. Telemetry parameters describing the status, configuration, and health of the spacecraft and subsystems are downlinked to the Command and Data Acquisition (CDA) Station and sent to the Satellite Operations Control Center (SOCC). Commands are received on board the spacecraft for controlling mission operations and managing expendable resource. This subsystem multiplexes telemetry data from sources throughout the spacecraft and converts analog signals to digital. The data is then formatted and synchronized in to the PCM serial data stream. The Block Diagram is shown in Fig. 8 below.

E. Minor Cycle Flag Generation.

In order to carry out different operation at different interval, timer flags are required. These flags are generated using the basic clock of 256 kHz.

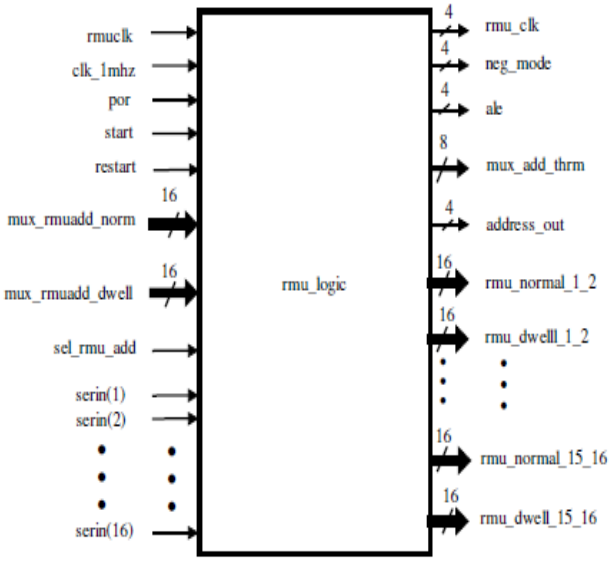

Fig. 7. Remote multiplexer unit logic.

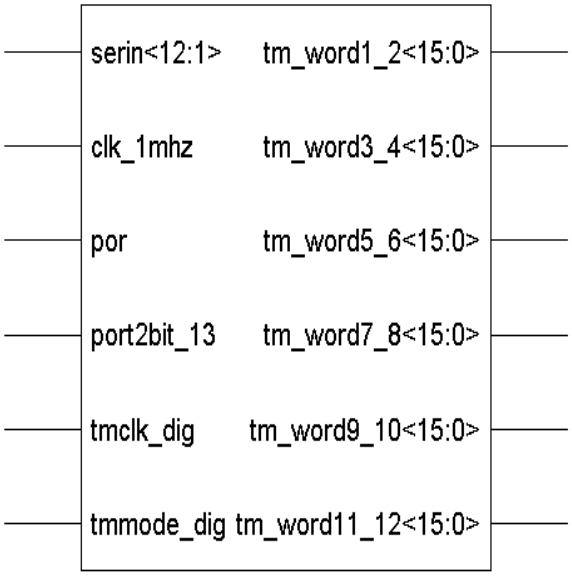

Fig. 8. Telemetry for digital words.

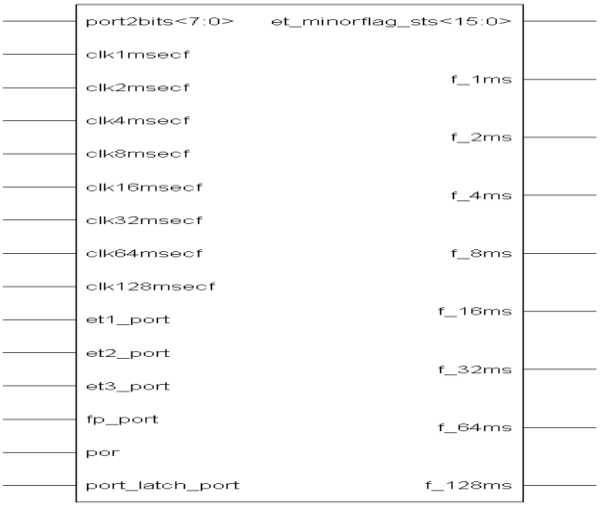

Fig. 9. Minor cycle flag generation.

F. Clock and Mode Generation.

This generates clocks of different frequencies from basic

256 kHz clock. The various clock required in different module is generated in this block.

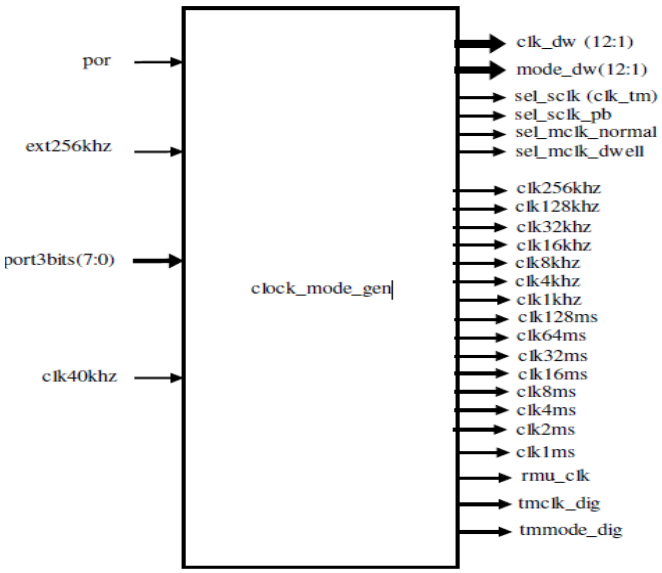

Fig. 10. Clock and mode generation.

G. *Telecommand Generation.*

This logic basically generates different commands for different operation. It has link1 and link2 data, which latches the data in 16 bits latches. The data is decoded and results the command in sequence.

IV. Simulation Results

The Design Implementation is done using Hardware Description Language (VHDL) and The Simulation and analysis of the Waveform is carried out using Modelsim.

The Waveform represents generation of required pulses at the arrival of start pulse from the processor and it generates start of conversion pulse after the arrival of the address generated by the address generator and the generated start of conversion pulse is fed to the ADC for conversion of analog signal to digital data along with the Main MUX address so as to acquire the data either normal data or dwell data.

The load pulse which is generated loads the digital data from ADC to latches and respectively to the processor. These data are read by the processor with reference to read signal from processor through IO Interface Block.

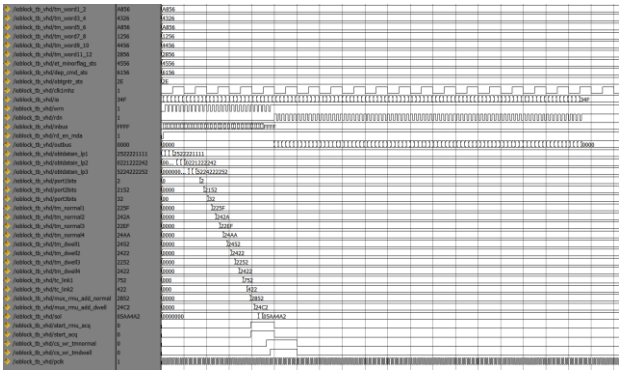

Fig. 11. Simulation result for IO interface.

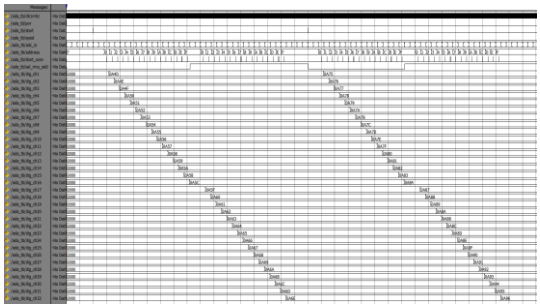

Fig. 12. Simulation result for analog data acquisition.

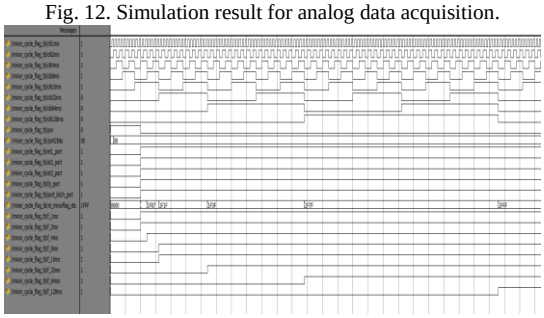

Fig. 13. Simulation result for minor cycle flag generation.

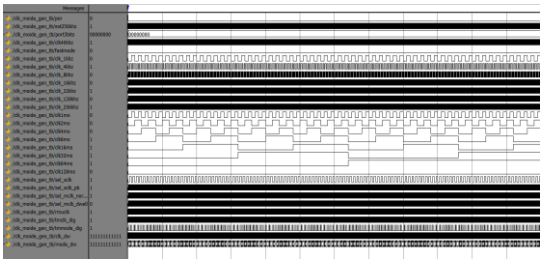

Fig. 14. Simulation result for clock and mode generation.

V. Conclusion and Future Enhancements

In this paper the architecture and function of Master Data Acquisition module have been highlighted. The objective of the project was to design and realize MDA using a hardware descriptive language.

The Functional blocks of MDA such as Analog Data Acquisition, IO Interface, Minor Flag Generation and Clock and mode generation is coded, simulated successfully.

The scope of the future development is the design and realization of the remaining Functional Blocks in Master Data Acquisition which is used in Telemetry Operations.

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