

# A New Hybrid 16-Bit×16-Bit Multiplier Architecture by $m:2$ and $m:3$ Compressors

Shima Mehrabi, Reza Faghii Mirzaee, Sharareh Zamanzadeh, and Amirhossein Jamalian

**Abstract**—Compressors are mostly used in multipliers to reduce partial products in a parallel manner. Firstly, this paper draw a comparison between the conventional  $m:2$  and  $m:3$  compressors. Secondly, a new hybrid 16-bit×16-bit multiplier is proposed in this paper with the aim of taking benefits from both kinds of compressors. The new design decreases the amount of carry signals by employing  $m:3$  compressors in the first stage. It also accelerates reducing partial products by using  $m:2$  compressors in the following stages. The second and third phases of multiplication are considered together in this paper. The synthesizable structural VHDL code is used to simulate and implement different architectures. Our investigations demonstrate that the new multiplier is the fastest one with reasonable power and area dissipations.

**Index Terms**—Compressor,  $m:2$  compressor,  $m:3$  compressor, full adder, half adder, hybrid architecture, multiplier, partial product reduction, ripple adder.

## I. INTRODUCTION

As the feature size of transistors keeps shrinking, more and more complicated signal processing systems are being implemented on a single nano-scale chip. In today's IC design industry, interconnections have become a serious challenge because they occupy a large amount of the chip area and lead to restrictions in placement and routing of logic elements [1]. They consume a lot of power and cause parasitic effects by increasing the number of connections inside a chip. Wire capacitance can contribute up to 70% of the total chip capacitance [2], [3]. On the other hand, faster logic elements and arithmetic units have always been in high demand.

Multiplication is considered as a rather complicated and time-consuming arithmetic operation. It is widely used in DSP algorithms such as filtering and Fourier transforms. It is also a fundamental computational unit in microprocessors, embedded systems, and crypto processors [4]-[7].

Multiplier architecture is divisible into three phases [8]: partial product generation phase; partial product reduction phase; and the final addition phase. At first, partial products are produced by multiplying each bit of the multiplicand with each bit of the multiplier. This phase results in a huge number of partial products in different bit-weight positions. As a

result, the partial product reduction is the most critical and time-consuming phase. All of the partial products must be accumulated up to the point where there are only two remaining partial products in each column. The final phase is the addition of these remaining partial products.

A compressor is simply an adder circuit. It takes a number of equally-weighted bits, adds them, and produces some sum signals. Compressors are commonly used with the aim of reducing and accumulating a large number of inputs to a smaller number in a parallel manner. Their main application is within a multiplier, where a huge number of partial products have to be summed up concurrently. The inner structure of compressors avoids carry propagation. Either there are not any carry signals or they do arrive at the same time of the internal values.

There are several different types of compressors. In general, an  $m:n$  compressor takes  $m$  input variables and returns  $n$  outputs. Carry signals are needed if the sum of input variables ( $\Sigma_{\text{Inputs}}$ ) is greater than the sum of outputs ( $\Sigma_{\text{Outputs}}$ ).  $m:2$  compressors are the most well-known ones due to their high bit-rate compression. However, their efficiency degree must be investigated inside a multiplier, not individually. On the other hand, it is shown in [9] that how  $m:3$  compressors might accelerate the phase of partial product reduction. Nevertheless, the third phase of multiplication is not taken into consideration in [9]. This paper takes the second and third phases into account, and presents a new hybrid multiplier architecture by the usage of  $m:2$  and  $m:3$  compressors. It combines the advantages of both kinds of compressors.

The rest of the paper is organized as follows: Section II includes a brief review of the conventional  $m:2$  and  $m:3$  compressors. Section III shows how compressors are connected together to form a 16×bit-16×bit multiplier. The proposed architecture is also presented in this section. Implementation results and comparisons are included in Section IV. Finally, Section V concludes the paper.

## II. THE CONVENTIONAL $m:2$ AND $m:3$ COMPRESSORS

Compressors are widely used in the second phase of a multiplier to accumulate partial products in a concurrent manner. Their inner structure avoids carry propagation. The conventional  $m:2$  and  $m:3$  compressors are briefly reviewed in this section.

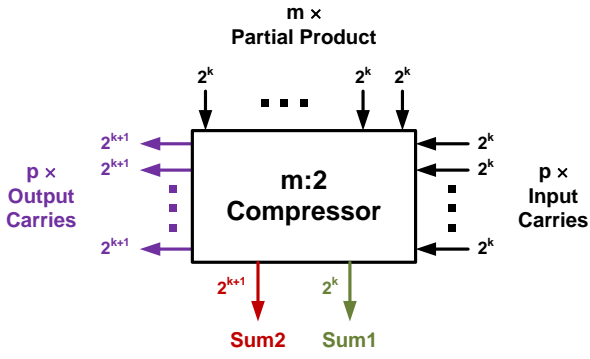
The overall structure of an  $m:2$  compressor is shown in Fig. 1, where the weights of the partial products are indicated by different colors. It takes  $m$  equally weighted input signals and returns two main outputs (Sum1 and Sum2). In addition, the  $m:2$  compressor requires  $p$  input and output carries. Equation 1 demonstrates that  $p=m-3$ .

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 Fig. 1. The overall structure of an  $m:2$  compressor.

$$\sum_{i=1}^2 \text{Outputs} + \sum_{i=1}^p \text{Output Carries} \quad (1)$$

$$= \sum_{i=1}^m \text{Partial Products} + \sum_{i=1}^p \text{Input Carries}$$

$$2^k + 2^{k+1} + p \times 2^{k+1} = (m + p) \times 2^k \quad (1.1)$$

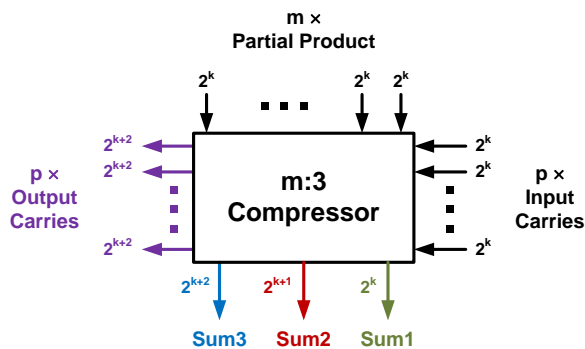
$$(2p + 3) \times 2^k = (m + p) \times 2^k \quad (1.2)$$

$$p = m - 3 \quad p \geq 0 \quad (1.3)$$

The overall structure of an  $m:3$  compressor is shown in Fig. 2. It produces one more main output signal (Sum3) than the  $m:2$  does. This additional output provides a higher range of output values. Therefore, the  $m:3$  compressor requires fewer carry signals than the  $m:2$  does. Generally, it needs  $\left\lfloor \frac{m-7}{3} \right\rfloor$

input and output carries (equation 2). Thus, for instance, 4:3, 5:3, 6:3, and 7:3 compressors do not need any carries at all, and 8:3, 9:3, and 10:3 ones require only one input/output carry. The fewer carry signals exist, the fewer interconnections are needed. On the other hand, the  $m:2$  compressors accumulate partial products quicker and produce fewer output Sums.

The inner structures of the  $m:2$  and  $m:3$  compressors are illustrated in Fig. 3 and Fig. 4, respectively. Tables I and II show that how many Half Adders (HA) and Full Adders (FA) are required to form the conventional compressors. The delay parameter of Half and Full Adders are considered as  $\tau_{HA}$  and  $\tau_{FA}$ . We assume that HAs are almost twice as fast as FAs ( $\tau_{FA} \approx 2 \times \tau_{HA}$ ).


 Fig. 2. The overall structure of an  $m:3$  compressor.

$$\sum_{i=1}^3 \text{Outputs} + \sum_{i=1}^p \text{Output Carries} \quad (2)$$

$$= \sum_{i=1}^m \text{Partial Products} + \sum_{i=1}^p \text{Input Carries}$$

$$2^k + 2^{k+1} + 2^{k+2} + p \times 2^{k+2} = (m + p) \times 2^k \quad (2.1)$$

$$(4p + 7) \times 2^k = (m + p) \times 2^k \quad (2.2)$$

$$p = \left\lfloor \frac{m-7}{3} \right\rfloor \quad p \geq 0 \quad (2.3)$$

To estimate how rapidly an  $m:n$  compressor accumulates partial products, its bit-rate compression is quantified by equation 3 [10], where the delay parameter is normalized by  $\tau_{HA}$ . The  $m:2$  compressors reduce partial products faster (Tables II and III), paying the price of having more hardware components and interconnections. Note that although the  $m:2$  compressors have higher bit-rate compression, the  $m:3$  compressors are internally faster because of their shorter critical path. Therefore, their rapidness has to be investigated within a practical multiplier block. In the following sections, their impact on a 16-bit-16-bit multiplier is examined.

$$\text{Bit-rate compression} = \frac{\log(m) - \log(n)}{\text{Delay}} \quad (3)$$

 TABLE I: SPECIFICATIONS OF THE CONVENTIONAL  $M:2$  COMPRESSORS

| Comp. | Delay by $\tau_{HA}$<br>(Normalized) | Bit-rate<br>Compression | #(In/Out)<br>Carries | #FA | #HA |
|-------|--------------------------------------|-------------------------|----------------------|-----|-----|
| 4:2   | 4                                    | 0.0753                  | 1                    | 2   | 0   |
| 5:2   | 6                                    | 0.0663                  | 2                    | 3   | 0   |
| 6:2   | 6                                    | 0.0795                  | 3                    | 4   | 0   |
| 7:2   | 8                                    | 0.0680                  | 4                    | 5   | 0   |
| 8:2   | 8                                    | 0.0753                  | 5                    | 6   | 0   |
| 9:2   | 8                                    | 0.0817                  | 6                    | 7   | 0   |
| 10:2  | 10                                   | 0.0699                  | 7                    | 8   | 0   |

 TABLE II: SPECIFICATIONS OF THE CONVENTIONAL  $M:3$  COMPRESSORS

| Comp. | Delay by $\tau_{HA}$<br>(Normalized) | Bit-rate<br>Compression | #(In/Out)<br>Carries | #FA | #HA |
|-------|--------------------------------------|-------------------------|----------------------|-----|-----|
| 4:3   | 4                                    | 0.0312                  | 0                    | 1   | 3   |
| 5:3   | 5                                    | 0.0444                  | 0                    | 2   | 1   |
| 6:3   | 5                                    | 0.0602                  | 0                    | 3   | 1   |
| 7:3   | 6                                    | 0.0613                  | 0                    | 4   | 0   |
| 8:3   | 7                                    | 0.0609                  | 1                    | 5   | 2   |
| 9:3   | 7                                    | 0.0682                  | 1                    | 6   | 1   |
| 10:3  | 8                                    | 0.0654                  | 1                    | 7   | 0   |

### III. MULTIPLIERS BY $M:2$ AND $M:3$ COMPRESSORS

A 16-bit×16-bit multiplier is exemplified in this paper to compare  $m:2$  and  $m:3$  compressors. The first multiplier is the one with only  $m:2$  compressors (Fig. 5). The second one is only composed of  $m:3$  compressors (Fig. 6). The second phase of both multipliers is made of three stages, where the unattached input carries are connected to the ground (GND). There are a large amount of interconnections within the first stage of the first multiplier (Fig. 5). On the other hand, there

are more remaining partial products in the second stage of the multiplier by  $m:3$  compressors (Fig. 6). The  $m:2$  compressors

produce fewer partial products in comparison with the  $m:3$  ones.

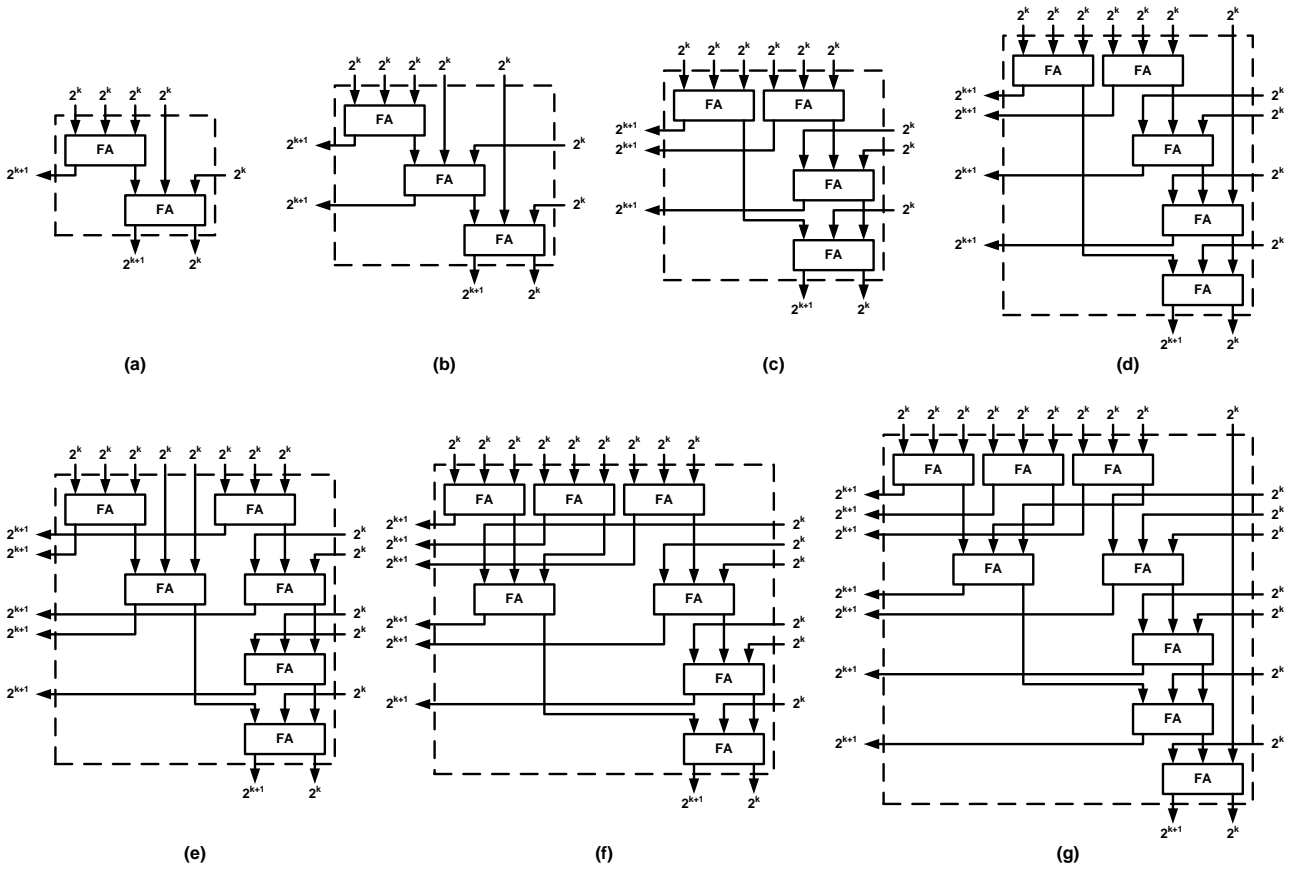


Fig. 3. The inner structure of the  $m:2$  compressor, (a) 4:2 [11], (b) 5:2 [12], (c) 6:2 [10], (d) 7:2 [13], (e) 8:2 [14], (f) 9:2 [15], (g) 10:2 [16].

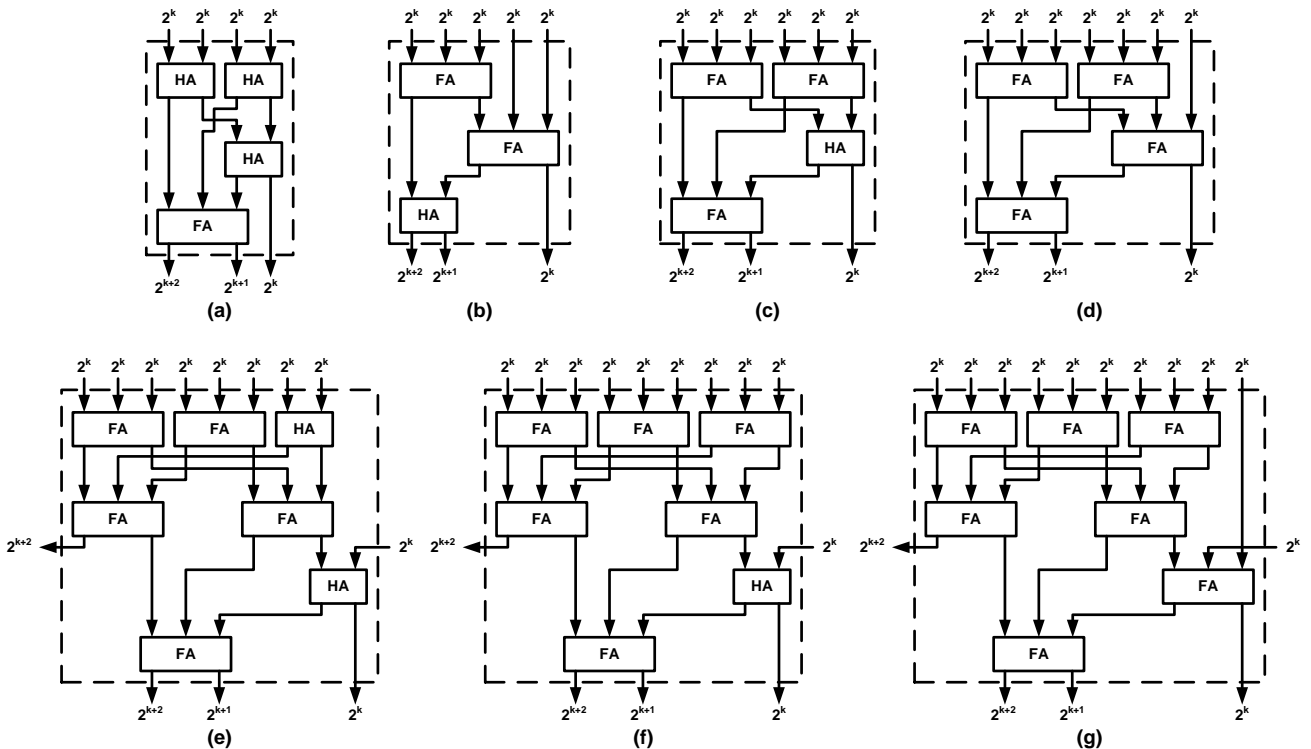


Fig. 4. The inner structure of the  $m:3$  compressor, (a) 4:3 [17], (b) 5:3 [18], (c) 6:3 [19], (d) 7:3 [20], (e) 8:3 [9], (f) 9:3 [9], (g) 10:3 [9].

The proposed 16-bit $\times$ 16-bit multiplier is depicted in Fig. 7. It is a hybrid architecture, which is made of both kinds of  $m:2$  and  $m:3$  compressors. The first stage is built by the  $m:3$  compressors in order to reduce carry signals and

interconnections subsequently. Then, the  $m:2$  compressors are exploited in the second stage to accelerate partial product reduction. As a result, the proposed design benefits from the strong points of both  $m:2$  and  $m:3$  compressors.

Output carries are always connected to the following compressors, situated in the next columns (Fig. 7). Although there are three partial products in the 21<sup>st</sup> column of the second stage, a 4:2 compressor is inserted in this column. The reason is to avoid four partial products in the next stage. If we had put a Full Adder in that position, there would have been four partial products in the same column of the third stage. The utilized 4:2 compressor absorbs the previous carry signal and prevents from sending it to the next stage. As a result, the second phase is completed in three stages (Fig. 7), the same as the way other ones do (Fig. 5 and Fig. 6).

Furthermore, the third phase of multiplication, final addition, directly affects the entire performance. This is due to the fact that the third phase might somehow fade away the parallelism of the second phase. In spite of some improving techniques such as Carry-Lookahead Adder (CLA) and Carry-Skip Adder (CSA), carry propagation cannot be entirely eliminated in the final phase. Therefore, the third phase is as important as the second one, and it cannot be ignored. To consider the worst case scenario, a simple ripple adder is considered in this paper for the final addition. Moreover, to reveal the importance of the third phase, simulations are performed twice: One time, the second phase is solely simulated and once again with considering the final ripple adder. Implementation results will be given in the next section.

It is also worth mentioning that although the  $m:2$  compressors have higher bit-rate compression, they might not necessarily result in higher speed for the entire multiplier. The reason is that despite the fact that an  $m:2$  compressor ( $5 \leq m \leq 10$ ) produces fewer partial products, they form a longer critical path compared to the equivalent  $m:3$  ( $5 \leq m \leq 10$ ) compressor. For example,  $\tau_{10:2} = \tau_{10:3} + \tau_{FA}$  (Fig. 3(g) and Fig. 4(g)). Thus, the speed of the whole multiplier depends on the critical path from the first stage to the last Full Adder of the final ripple adder.

#### IV. IMPLEMENTATION RESULTS

All of the multipliers are implemented by structural VHDL code and synthesized by Synopsys synthesis tool without performing any specific optimization. The synthesis process is carried out with 90nm CMOS technology in 1V power supply. As mentioned earlier, the initial simulation results do not include the ripple adder (Table III). In this case, the proposed multiplier is the slowest one. However, when the final ripple adder is also applied (Table IV), the new hybrid architecture operates 0.22% and 5.12% faster than the first and second multiplier, respectively. It also consumes 7.73% less power than the multiplier by  $m:2$  compressors due to the elimination of carry signals in the first stage. Eventually, the new design occupies 1.2% less area than the multiplier by  $m:3$  compressors.

TABLE III: THE DELAY PARAMETER WITHOUT CONSIDERING THE RIPPLE ADDER

| Multiplier        | by only $m:2$ Compressors | by only $m:3$ Compressors | Proposed Architecture |
|-------------------|---------------------------|---------------------------|-----------------------|
| Data Arrival Time | 1.60 nsec                 | 1.40 nsec                 | 2.61 sec              |

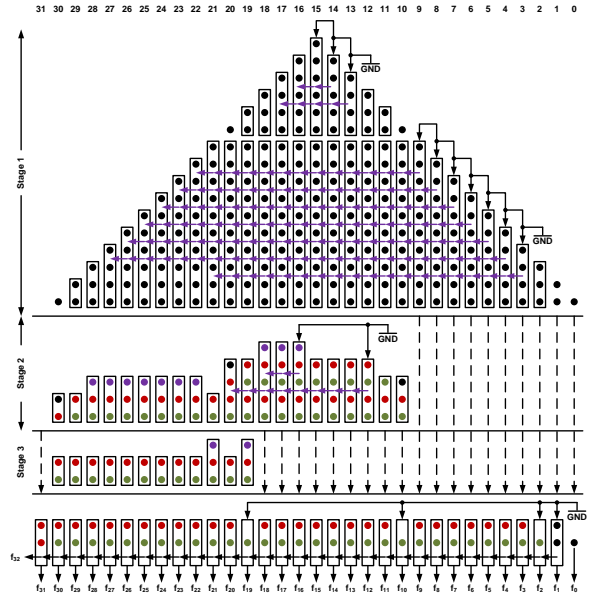


Fig. 5. 16-Bit x 16-bit multiplier by only  $m:2$  compressors.

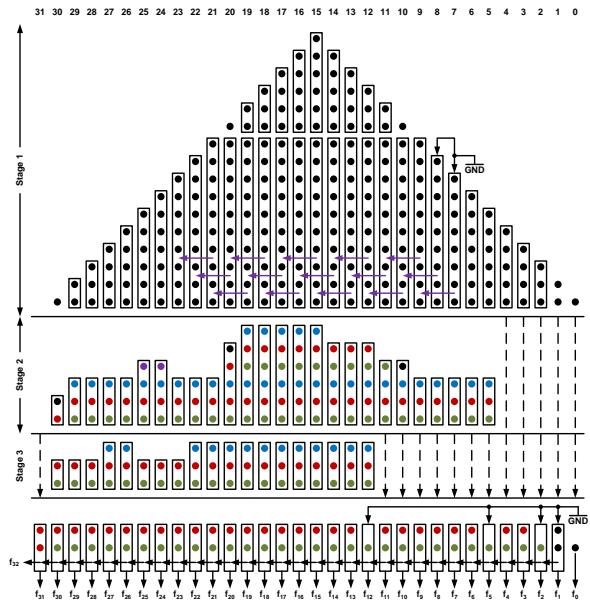


Fig. 6. 16-bit x 16-bit multiplier by only  $m:3$  compressors.

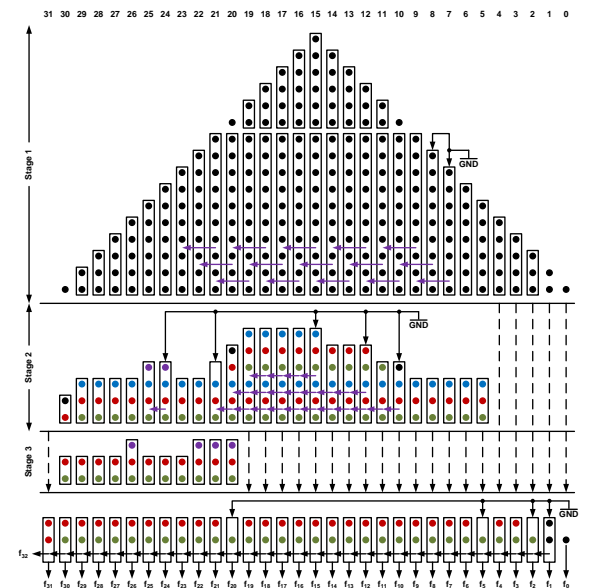


Fig. 7. The proposed hybrid 16-bit x 16-bit multiplier by  $m:2$  and  $m:3$  compressors.

TABLE IV: IMPLEMENTATION RESULTS WITH THE FINAL RIPPLE ADDER

| Multiplier             | by only $m:2$<br>Compressors | by only $m:3$<br>Compressors | Proposed<br>Architecture |
|------------------------|------------------------------|------------------------------|--------------------------|
| Data Arrival Time      | 4.69 nsec                    | 4.46 nsec                    | 4.45 nsec                |
| Total Cell Area        | 4340.9 $\mu\text{m}^2$       | 4428.4 $\mu\text{m}^2$       | 4375.4 $\mu\text{m}^2$   |
| Cell Internal Power    | 1079.3 $\mu\text{W}$         | 1002.9 $\mu\text{W}$         | 1019.3 $\mu\text{W}$     |
| Net Switching<br>Power | 542.16 $\mu\text{W}$         | 462.22 $\mu\text{W}$         | 500.22 $\mu\text{W}$     |
| Total Dynamic<br>Power | 1621.4 $\mu\text{W}$         | 1465.2 $\mu\text{W}$         | 1519.5 $\mu\text{W}$     |
| Cell Leakage Power     | 8.4090 $\mu\text{W}$         | 8.4990 $\mu\text{W}$         | 8.4368 $\mu\text{W}$     |

## V. CONCLUSION

The proposed hybrid 16-bit $\times$ 16-bit multiplier is an excellent trade-off between the ones which use only  $m:2$  or  $m:3$  compressors. While it is the fastest design, it consumes less power than one of the designs, and it occupies less area than the other one. The usage of  $m:3$  compressors leads to fewer interconnections. On the other hand,  $m:2$  compressors reduce partial products quicker. Their combination is considered in the new design. Another important conclusion is that although the second phase is known to be the most critical one, the correct analysis must include the second and third phases together.

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