# Junctionless CMOS Transistors with Independent Double Gates

A. Kamath, Z. X. Chen, N. Shen, X. Li, N. Singh, G. Q. Lo, and D.-L. Kwong

***Abstract*—Scaling is getting challenging with every technology node. Implant process requirements for defining conformal junctions in 3D device are very stringent. In addition, defining gate over topography is limited by lithography. Our solution to these problems is a novel junction-less FiNFET like transistor. Unlike conventional FiNFET the gate definition in this device is lithography independent. The fabricated NMOS and PMOS shows good transistor characteristics: $I_{ON}$ =52.3 uA/um, ION/IOFF ratio = $10^7$, SS = 92mV/dec for NMOS and ION =15.4 uA/um, ION/IOFF ratio = $10^5$, SS = 90mV/dec for PMOS. We also show inverter VTC characteristics fabricated using this NMOS and PMOS.**

***Index Terms*—CMOS, junctionless, independent gates**

## I. Introduction

Short channel effects in planar CMOS transistors are a major hurdle for scaling. The main reason for Short channel effects in scaled transistors is poor gate control. To counter this, the current focus is to have Channel in the third dimension in the form of vertical Fin or Nano wires, controlled by gate around the channel. Hence FinFET [1], tri-gate MOSFET [2], and gate-all-around (GAA) Nano wire MOSFET [3], [4] have been researched extensively as solutions. Though promising from a scalability perspective, all these devices might suffer from fabrication or reliability related issues. For example, the FinFET requires gate to be patterned across the fin. Three-dimensional devices also require doping to be conformal, increasing the complexity of junction formation, which, in any case, becomes more challenging with every new technology node [6]. Junction-less devices have started to gain research focus to tackle junction related issues [7]-[9].

In this work, we experimentally demonstrate a junction-less independent gate transistor. The process flow designed helps to keep the cost low owing to lesser process steps and also mitigates several problems associated with other devices with similar architecture. This device has a channel in the form of a vertical Fin; the current is modulated by two independent gates formed on the side walls. Unlike conventional transistors, this device is free from doped-junctions, which alleviates the need for precise conformal doping required for other junction based 3D devices.

In our first demonstration of N and P channel transistors presented here, we find the device exhibits good transistor characteristics, which makes it suitable for ULSI integration.

Manuscript received June 6, 2012; revised September 5, 2012.

The authors are with Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), CO 117685 Singapore (e-mail: kamathar@ ime.a-star.edu.sg).

## II. Device Fabrication

We started the fabrication using standard 8" p-type boron doped (1E15 cm-3) SOI wafers with 1140A top silicon on 1450A BOX. Wafers were first implanted with phosphorus for N channel devices and boron for P channel devices through a resist mask (to isolate other areas) and annealed to yield uniform doping concentrations of 5E17cm-3 in both regions, a number obtained through TCAD simulations. Silicon nitride was deposited using LPCVD process on thin 30A pad oxide, which was thermally grown. Fins were patterned by DUV lithography on silicon nitride which later acted as a hard mask for etch. The nitride hard mask and the underlying silicon were both dry-etched. Gate oxide of thickness 45Å was grown in dry oxygen, which was followed by deposition of amorphous silicon as gate material. Gate silicon was then polished to isolate the two gates from top. It was followed by BF2 implantation for N channel device and Phosphorus for P channel devices into the gate and then activation. Hence the channel and the gate are of opposite doping. During the gate implant, channel was protected by SiN hard mask. It was followed by active area etch. Then, 4000A pre-metal dielectric was deposited followed by contact hole etching and standard metallization processes. TEM of the final device across the FIN showing channel dimensions and two independent gates is shown in Figure

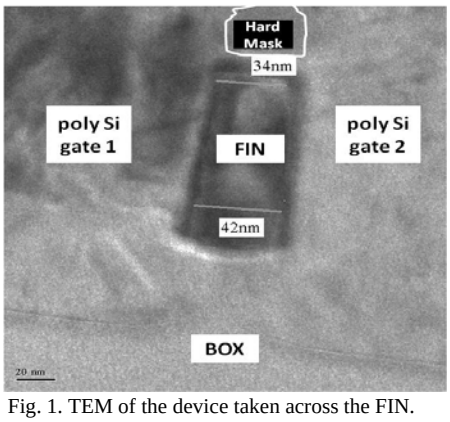



Fig. 1. TEM of the device taken across the FIN.

## III. Electrical Results

We characterized the devices with independent gates by applying different fixed potentials on one gate and varying the other and with gates shorted together to see the impact of second gate. Shown in Fig. 2 are the Id-Vg characteristics of NMOS and PMOS device with slit doping of 5E17cm-3,

DOI: 10.7763/IJIEE.2013.V3.254

channel (FIN) width of 40nm (Using average of top and bottom width of the FIN) with two gates tied. NMOS device shows good electrical characteristics with a ION of 52 uA/um with SS = 92mV/dec and has a threshold voltage of 0.45V. PMOS device has relatively high threshold value of 1V and a relatively low ION of 15.4 uA/um with a SS of 90mV/dec. The reason higher threshold voltage in PMOS is because of Boron out diffusion (from channel) during sacrificial oxidation done to make the FIN narrower, (Process flow followed is channel doping first followed by FIN etch and Sacrificial oxidation to make the FIN narrow) this out diffusion of boron causes relative lower doping in P channel resulting in increased depletion region in the channel from the N type gate around the channel. The relative lower doping in the P channel is also the cause for Low ION as in a junctionless device the ON current is directly proportional to the dopant density. An ON current is normalized to FIN height.

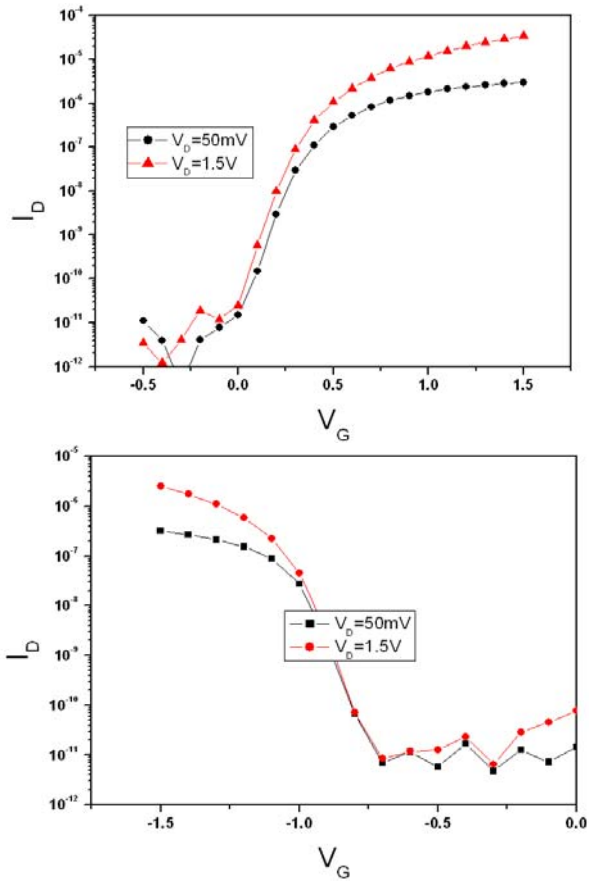



Fig. 2. Id-Vg Characteristics of NMOS and PMOS device respectively.

Fig. 3 shows the Id-Vd characteristics of the transistors. The drain Voltage shown is absolute value. The fixed drain voltages were varied till 2V in case of PMOS because of its high threshold voltage. Fig 4 Show the Voltage transfer characteristics of Inverter. This inverter was fabricated using the NMOS and PMOS described in this work. It shows a transition voltage of around 0.4V. This is expected as the NMOS device is stronger compared to PMOS. The voltage swing is not full rail voltage due to relatively higher OFF current in PMOS transistor and High drain extension resistance. We need to further optimize this by fine tuning the implant condition for P channel implant. Extension resistance can be changed by careful layout planning.

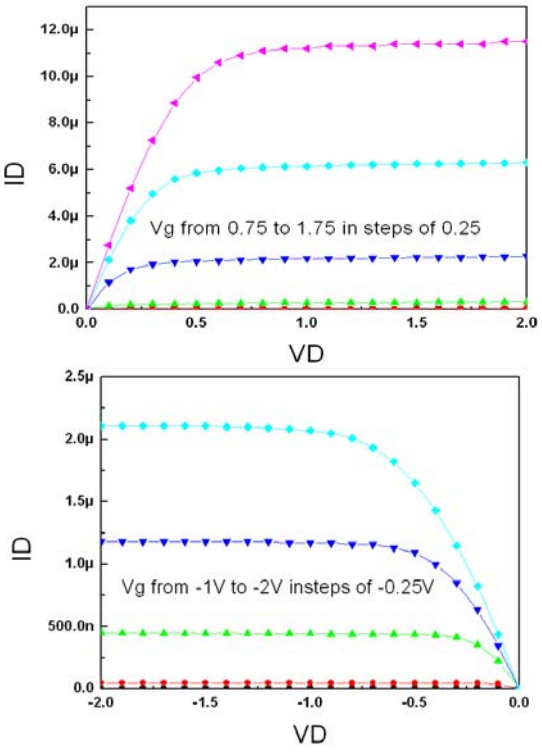



Fig. 3. Id-Vd characteristics of NMOS and PMOS device respectively.

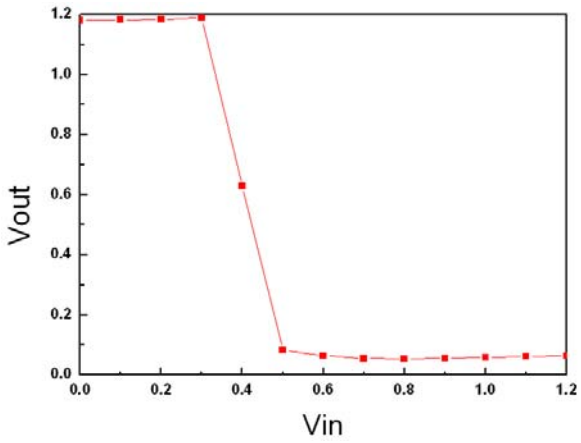



Fig. 4. Voltage transfer characteristics of inverter.

## IV. Conclusion

In this work we present a novel Junction less CMOS transistors fabricated on SOI wafer using conventional CMOS Processes. The process flow used makes this device low cost owing to simpler and reduced number of process steps. This flow also helps to mitigate lithography restrictions plaguing other similar independent devices during gate definition. This initial work shows good NMOS characteristics high ION and ION/IOFF ratio. While PMOS characteristic exhibits high threshold voltage, it can easily be rectified by fine tuning the P channel implant. In addition to above, we also present Inverter voltage transfer characteristics. The simple process flow of this device and its junctionless nature along with good electrical characteristics will make it a good contender for future USLI.

## REFERENCES


[1] C. Y. Chang *et al*. "A 25-nm gate-lenth FinFET transistor module for 32nm node," *IEDM Tech. Dig*, pp. 1-4, 2009.

[2] S. Xin, L. Qiang, V. Moroz, H. Takeuchi, G. Gebara, J. Wetzel, S. Ikeda, C. Shin, and T. J. K. Liu, "Tri-Gate Bulk MOSFET Design for CMOS Scaling to the End of the Roadmap," *IEEE Electron Device Lett*, pp. 491-493, 2008.

[3] N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, C. H. Tung, K. M. Hoe, S. R. Omanpuliyur, D. Tripathi, A. O. Adeyeye, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Ultra-Narrow Silicon Nanowire Gate-All-Around CMOS Devices: Impact of Diameter, Channel-Orientation and Low Temperature Device Performance," *IEDM Tech. Dig*, pp. 1-4, 2006.

[4] B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L Kwong, "Vertical silicon-nanowire formation and gate-all-around MOSFET," *IEEE Electron Device Lett*, no 29, 2008.

[5] T. Honda, M. Kawashima, Y. Sekine, K. Yamazoe, and E. Sakamotom, "Hyper-NA imaging in ArF immersion lithography," In *Microprocesses and Nanotechnology Conference*. 2005.

[6] S. Borkar, "Design perspectives on 22nm CMOS and beyond," *IEDM Tech. Dig*, pp. 93-94, 2009.

[7] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'neill, A. Blake, M. White, A.M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nature Nanotechnology*, 2010.

[8] A. M. Ionescu, "Electronic Devices:Nanowire transistors made easy," *Nature Nanotechnology*, 2010.

[9] C. W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J. P. Colinge, "High-Temperature Performance of Silicon Juntionless MOSFETs," *IEEE Tran. Electron Devices*, 2010.


.