Voltage-Mode Universal Filter Employing Two Plus-Type DDCCs

Hua-Pin Chen, Kuo-Wei Huang, and Tsung-Yu Liu

***Abstract*—This paper introduces a voltage-mode universal filter with three inputs and four outputs employing two plus-type differential difference current conveyors (DDCCs), two grounded capacitors and two resistors. The proposed circuit can act as a high-input impedance multifunction voltage-mode filter with single input and four outputs and can simultaneous realization of voltage-mode lowpass, highpass and two bandpass filter responses from the four output terminals, respectively, without any component choice conditions. On the other hand, it also can act as a universal voltage-mode filter with three inputs and a single output and can realize all five different generic filtering responses from the same configuration without any component matching conditions. The circuit dose not require inverting-type voltage single to realize all the filtering functions. Active and passive sensitivity performances are low. HSPICE simulation results using TSMC 0.18μm 1P6M CMOS process technology and ±0.9V supply voltages validate the theoretical predictions.**

***Index Terms*—Active filters, voltage-mode; DDCC, analog electronics.**

I. INTRODUCTION

As a current-mode active device, the differential difference current conveyor (DDCC) has the advantages of both the second generation current conveyor (such as large signal bandwidth, great linearity, wide dynamic range) and the differential difference amplifier (such as high input impedance and arithmetic operation capability) [1]. Since the addition and subtraction operations of voltage-mode signals need the realization, respectively. The DDCC becomes very attractive to be used in the design of voltage-mode filters. This is due to the fact that the addition and subtraction operations for voltage signals can be performed easily by DDCC [1–7]. Voltage-mode active filters with high-input impedance are of great interest because several cells of this kind can be directly connected for implementing higher order filters [3–11]. In 2003, Chang and Chen proposed a universal voltage-mode filter with three inputs and a single output [2]. The circuit can realize all five different generic filtering responses but only highpass (HP) and bandpass (BP) responses have the advantage of high input impedance. In 2004, Horng et al. proposed a multifunction filter with a single input and three outputs [3]. The circuit can realize HP, BP and lowpass (LP) responses, simultaneously. However, it suffers from orthogonal tunable of the resonance angular frequency ω_o and quality factor Q. In 2005, Ibrahim et al. proposed two single DDCC biquads with high input impedance and minimum number of passive elements [4]. The HP, BP or LP filter responses cannot be realized in the same configuration. In 2007, Chiu and Horng proposed a universal voltage-mode filter with three inputs and a single output [5]. The circuit has high-input and low-output impedance advantages but it uses three plus-type DDCCs. In the same year, Chen proposed a universal voltage-mode filter based on two plus-type DDCCs [6]. The proposed configuration suffers from high-input impedance. In 2010, Chen proposed another multifunction voltage-mode filter with single input and four outputs [7]. The circuit can realize inverting HP, inverting BP, non-inverting LP and non-inverting BP filter responses, simultaneously. However, the three inputs and a single output can not be used in the same configuration. In this paper, a new voltage-mode universal biquadratic circuit with three inputs and four outputs is presented. The proposed configuration employs two DDCCs, two grounded capacitors and two resistors. Either three inputs and single output or single input and four outputs can be used in the same configuration. The biquadratic filter needs neither an inverting-type voltage input signal nor any critical component-matching conditions to realize all five generic filtering responses. The non-ideality analysis of the proposed filter is given. In addition, the parasitic impedance effects of the active elements on the proposed filter are investigated. It still enjoys low active and passive sensitivity performances.

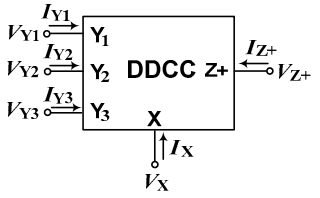

Fig. 1. Electrical symbol of plus-type DDCC.

II. CIRCUIT DESCRIPTION

The plus-type DDCC, whose electrical symbol is shown in Fig. 1, is a five-terminal analog building block. The block diagram representing the implementation of the three inputs and four outputs filtering circuit is shown in Fig. 2. It consists of two lossless integrators and three summers. From the diagram in Fig. 2, the implementation of the voltage-mode universal biqaudratic circuit is shown in Fig. 3. It employs two DDCCs, two grounded capacitors and two resistors. The use of grounded capacitors is attractive from monolithic integration point of view because grounded capacitor circuits

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can compensate for the stray capacitances at their nodes [12]. The plus-type DDCC is a five-terminal analog building block. All the Y_1, Y_2 and Y_3 terminals of DDCC are high impedance terminals, since they are connected to gates of MOS devices in actual implementation, whereas the port X is low impedance terminal [1]. Similarly the port Z+ exhibits high impedance since it is connected to the output stage of current mirror. Using standard notation, the port relations of an ideal DDCC can be characterize by $I_{Y1}=I_{Y2}=I_{Y3}=0$, $V_X=V_{Y1}-V_{Y2}+V_{Y3}$ and $I_{Z+}=I_X$ [1]. Derived by each nodal equation of the proposed, the input-output relationship matrix form of Fig. 3 can be expressed as

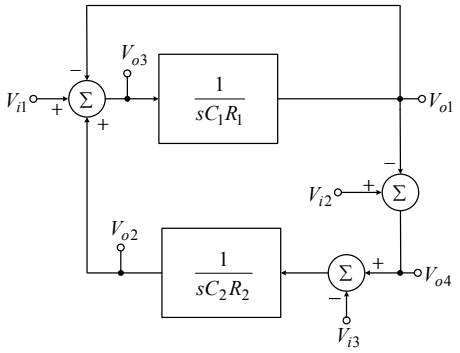

Fig. 2. Block diagram of the proposed filtering circuit.

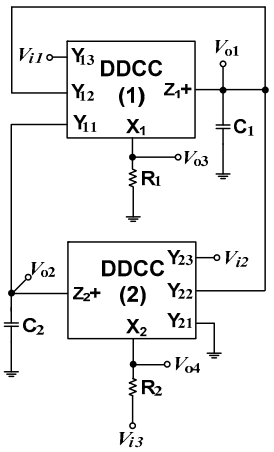

Fig. 3. The proposed tunable voltage-mode multifunction biquadratic filter.

$$\begin{bmatrix} sC_1 & 0 & -G_1 & 0 \\ 0 & sC_2 & 0 & -G_2 \\ 1 & -1 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{o1} \\ V_{o2} \\ V_{o3} \\ V_{o4} \end{bmatrix} = \begin{bmatrix} 0 \\ -G_2V_{i3} \\ V_{i1} \\ V_{i2} \end{bmatrix} \quad (1)$$

where $G_1 = \frac{1}{R_1}$ and $G_2 = \frac{1}{R_2}$

From (1), if $V_{i1}=V_{in}$ (the input voltage signal) and $V_{i2}=V_{i3}=0$ (namely, the resistors R_1 and R_2 are grounded), then the following four output voltages can be derived as

$$\frac{V_{o1}}{V_{in}} = \frac{sC_2R_2}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \quad (2)$$

$$\frac{V_{o2}}{V_{in}} = \frac{-1}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \quad (3)$$

$$\frac{V_{o3}}{V_{in}} = \frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \quad (4)$$

$$\frac{V_{o4}}{V_{in}} = \frac{-sC_2R_2}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \quad (5)$$

Thus, the non-inverting bandpass, inverting lowpass, non-inverting highpass and inverting bandpass filter responses are obtained at the node voltages, V_{o1}, V_{o2}, V_{o3} and V_{o4}, respectively. Note that the input signal, $V_{i1}=V_{in}$, is connected to the high input impedance input node of the DDCC(1) (the Y_3 port of the DDCC(1)). So the circuit enjoys the advantage of having high input impedance, leading to cascadability at the input port. Moreover, the use of only grounded capacitors is particularly attractive for integrated circuit implementation.

On the other hand, from (1), the output voltage V_{o4} can be derived as

$$V_{o4} = \frac{-sC_2R_2V_{i1} + (s^2C_1C_2R_1R_2 + sC_2R_2)V_{i2} + V_{i3}}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \quad (6)$$

Depending on the voltage status of V_{i1}, V_{i2} and V_{i3} in the numerator of (6), one of the following five filter functions is realized:

(i) lowpass (LP): $V_{i1}=V_{i2}=0$ and $V_{i3}=V_{in}$

(ii) bandpass (BP): $V_{i2}=V_{i3}=0$ and $V_{i1}=V_{in}$

(iii) highpass (HP): $V_{i3}=0$ and $V_{i1}= V_{i2}=V_{in}$

(iv) bandreject (BR): $V_{i1}=V_{i2}=V_{i3}=V_{in}$

(v) allpass (AP): $0.5V_{i1}=V_{i2}=V_{i3}=V_{in}$

Note that there is also no need of any component matching conditions and inverting type voltage input signals to realize all of the filter responses.

Obviously, the proposed circuit can act as a multifunction voltage-mode filter with single input and four outputs and it can also act as a universal voltage-mode filter with three inputs and a single output, too. Therefore, the proposed circuit is more versatile than those with a single input and three outputs or with three inputs and a single output. The denominator polynomial of the transfer functions of the proposed filter can be obtained as

$$D(s) = s^2C_1C_2R_1R_2 + sC_2R_2 + 1 \quad (7)$$

From (7), the resonance angular frequency ω_o, the quality factor Q and bandwidth can be given as

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (8)$$

$$Q = \sqrt{\frac{R_1C_1}{R_2C_2}} \quad (9)$$

$$BW = \frac{\omega_o}{Q} = \frac{1}{R_1C_1} \quad (10)$$

From (8) and (9), it can be seen that the resonance angular frequency can be independently adjusted from the bandwidth, by varying C_2 or R_2. Also, the passive ω_o and Q sensitivities are all calculated as 0.5 in magnitude.

III. Effect of Non-Idealities

Taking the non-idealities from frequency dependence of

internal voltage and current transfers of the DDCC into account, the relationship of the terminal voltages and currents can be rewritten as $V_X = \beta_a(s)V_{Y1} - \beta_b(s)V_{Y2} + \beta_c(s)V_{Y3}$ and $I_{Z+} = \alpha(s)I_X$, where $\alpha(s)$ and $\beta_n(s)$ (n=a, b, c) represent the frequency transfers of the internal current and voltage followers of the DDCC. They can be approximated by the first order of low-pass functions [13].

$$\alpha(s) = \frac{\alpha}{1+\frac{s}{2\pi f_{\alpha_m}}} \tag{11}$$

$$\beta_n(s) = \frac{\beta_n}{1+\frac{s}{2\pi f_{\beta_n}}}, \text{ for n=a, b, c} \tag{12}$$

In which $\alpha = 0.9999$, $\beta_a = 1.0000$, $\beta_b = 0.9999$, $\beta_c = 1.0000$ and using TSMC 018 um 1P6M CMOS process technology HSpice simulation with the parameters of lever 49 is performed. For frequencies much less than the f_{3dB} of DDCC, all $\alpha(s)$ and $\beta_n(s)$ are real quantities of magnitudes slightly less than or equal to one. Assuming that the circuit works at frequencies much less than the corner frequencies of $\alpha(s)$ and $\beta_n(s)$, namely, $\alpha(s) = \alpha = 1 - \varepsilon_i$ and $|\varepsilon_i| << 1$ denotes the current tracking error and $\beta_n(s) = \beta_n = 1 - \varepsilon_v$ and $|\varepsilon_i| << 1$ denotes the voltage tracking error of the DDCC. Taking into account the non-idealities, (2) to (5) can be rewritten as follows.

$$\frac{V_{o1}}{V_{in}} = \frac{\alpha_1\beta_{c1}sC_2R_2}{s^2C_1C_2R_1R_2 + \alpha_1\beta_{b1}sC_2R_2 + \alpha_1\alpha_2\beta_{a1}\beta_{b2}} \tag{13}$$

$$\frac{V_{o2}}{V_{in}} = \frac{-\alpha_1\alpha_2\beta_{c1}\beta_{b2}}{s^2C_1C_2R_1R_2 + \alpha_1\beta_{b1}sC_2R_2 + \alpha_1\alpha_2\beta_{a1}\beta_{b2}} \tag{14}$$

$$\frac{V_{o3}}{V_{in}} = \frac{s^2C_1C_2R_1R_2 + (\alpha_1\beta_{b1}sC_2R_2 + \alpha_1\alpha_2\beta_{a1}\beta_{b2})(1-\beta_{c1})}{s^2C_1C_2R_1R_2 + \alpha_1\beta_{b1}sC_2R_2 + \alpha_1\alpha_2\beta_{a1}\beta_{b2}} \tag{15}$$

$$\frac{V_{o3}}{V_{in}} = \frac{s^2C_1C_2R_1R_2 + (\alpha_1\beta_{b1}sC_2R_2 + \alpha_1\alpha_2\beta_{a1}\beta_{b2})(1-\beta_{c1})}{s^2C_1C_2R_1R_2 + \alpha_1\beta_{b1}sC_2R_2 + \alpha_1\alpha_2\beta_{a1}\beta_{b2}}$$

$$\approx \frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2 + \alpha_1\beta_{b1}sC_2R_2 + \alpha_1\alpha_2\beta_{a1}\beta_{b2}} \tag{16}$$

$$\frac{V_{o4}}{V_{in}} = \frac{-\alpha_1\beta_{c1}\beta_{b2}sC_2R_2}{s^2C_1C_2R_1R_2 + \alpha_1\beta_{b1}sC_2R_2 + \alpha_1\alpha_2\beta_{a1}\beta_{b2}} \tag{17}$$

The non-ideal resonance angular frequency ω_o and quality factor Q are obtained by

$$\omega_0 = \sqrt{\frac{\alpha_1\alpha_2\beta_{a1}\beta_{b2}}{R_1R_2C_1C_2}} \tag{18}$$

$$Q = \frac{1}{\beta_{b1}}\sqrt{\frac{\alpha_2\beta_{a1}\beta_{b2}R_1C_1}{\alpha_1R_2C_2}} \tag{19}$$

The active and passive sensitivities are derived to be

$$S^{\omega_o}_{\alpha_1,\alpha_2,\beta_{a1},\beta_{b2}} = -S^{\omega_o}_{R_1,R_2,C_1,C_2} = \frac{1}{2} \tag{20}$$

$$S^{Q}_{\alpha_2,\beta_{a1},\beta_{b2}} = S^{Q}_{R_1,C_1} = -S^{Q}_{\alpha_1} = -S^{Q}_{R_2,C_1} = \frac{1}{2} \tag{21}$$

$$S^{Q}_{\beta_{b1}} = -1 \tag{22}$$

From the above it can be realized that even under non-ideal current and voltage gains of the DDCCs the active and passive sensitivities remain less than or equal to one in magnitude.

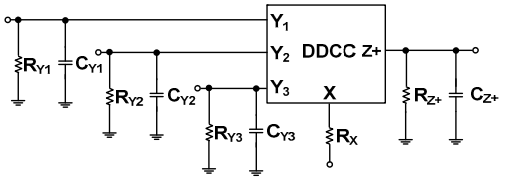

Fig. 4. Block diagram of DDCC symbol along with its parasitic elements.

IV. Parasitic Impedance Effects

The former equations from (2) to (6) have been obtained by considering ideal description of DDCCs, all the three Y terminals exhibit an infinite input resistance. The port X exhibits zero input resistance and the port Z+ shows an infinite output resistance. Practically when implementing the active element using transistors, these resistances assume some finite value depending upon the device parameters. Similarly, the high frequency effects also need to be accounted for by assuming capacitances at these ports. The non-ideal DDCC symbol showing various parasitic is shown in Fig. 4. It is shown that the port X exhibits of low value parasitic serial resistance R_X, the ports Y exhibit of high value parasitic resistance R_Y, and the port Z+ exhibits of high value parasitic resistance R_{Z+} in parallel with low value capacitor C_{Z+}. It is to be noted that the proposed circuit employs resistors at X terminals of the DDCCs; therefore, most of the parasitic R_X can be easily merged. To account for these non-ideal sources, the proposed circuit in Fig. 3 can be redrawn as Fig. 5. Note that in Fig. 5 all the grounded capacitors are connected at Z+ terminals of DDCCs to absorb shunt parasitic capacitances at Z+ terminals of DDCCs. Also, we used two grounded resistors at all X terminals of DDCCs to absorb series parasitic resistances at X terminals of DDCCs. Reanalysis of the proposed circuit, (2) to (5) can be rewritten as follows.

$$\frac{V_{o1}}{V_{in}} = \frac{n_1 s}{s^2 + n_1 s + n_1 n_2} \tag{23}$$

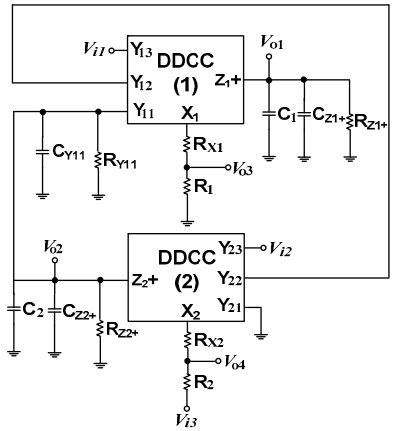

Fig. 5. The proposed voltage-mode universal biquadratic filter including parasitics.

$$\frac{V_{o2}}{V_{in}} = \frac{-n_1 n_2}{s^2 + n_1 s + n_1 n_2} \quad (24)$$

$$\frac{V_{o3}}{V_{in}} = \frac{H_1 s^2}{s^2 + n_1 s + n_1 n_2} \quad (25)$$

$$\frac{V_{o4}}{V_{in}} = \frac{-H_2 n_1 s}{s^2 + n_1 s + n_1 n_2} \quad (26)$$

where

$$H_1 = \frac{R_1}{R_1 + R_{X1+}} \quad (27)$$

$$H_2 = \frac{R_2}{R_2 + R_{X2+}} \quad (28)$$

$$n_1 = \frac{1}{R_1^{'}}\left(\frac{sR_{Z1+}}{1 + sR_{Z1+}C_1^{'}}\right) \quad (29)$$

$$n_2 = \left(\frac{1}{R_2^{'}}\right)\frac{sR_{2p}}{1 + sR_{2p}C_2^{'}} \quad (30)$$

$C_1^{'} = C_1 + C_{Z1+}$, $C_2^{'} = C_2 + C_{Z2+} + C_{Y11}$, $R_1^{'} = R_1 + R_{X1+}$,

$R_2^{'} = R_2 + R_{X2+}$ and $R_{2p} = R_{Z2+} // R_{Y11}$

Equations (29) and (30) can be rewritten as

$$n_1 = \left(\frac{1}{R_1^{'}C_1^{'}}\right)\left(\frac{s}{s + \omega_1}\right) \quad (31)$$

$$n_2 = \left(\frac{1}{R_2^{'}C_2^{'}}\right)\left(\frac{s}{s + \omega_2}\right) \quad (32)$$

where

$$\omega_1 = \frac{1}{R_{Z1+}C_1^{'}} \text{ and } \omega_2 = \frac{1}{R_{2p}C_2^{'}} \quad (33)$$

Equations (31) and (32) illustrate that the effects of the parasitic elements are dependent on two parasitic poles yielded by the non-idealities of the DDCCs. For close to ideal operation at high frequencies, the frequency of operation should be larger than ω_1 and ω_2. The frequency range of the proposed configuration should be restricted to the following conditions [13].

$$f \le f_H = 0.1 \times \min\{f_1,\ f_2\} \quad (34)$$

V. Simulation Results

Finally, to verify the theoretical prediction of the proposed biquadratic filter, a simulation using HSpice simulation with TSMC 0.18 μm 1P6M CMOS process technology was performed and the CMOS implementation of the DDCC is shown in Fig. 6 [4]. The dimensions of MOS transistors used in implementation of the DDCC are given in Table I. The supply voltages are V_{DD}=-V_{SS}=0.9V, and the biasing voltages are V_{B1}=-0.1V and V_{B2} =-0.36V. The voltage follower and current follower frequency responses of DDCC are, respectively, shown in Figs. 7 and 8 which are obtained more than 100MHz. The f_{-3dB} frequencies for the voltage and current transfers are summarized in Table II. The frequency response of the output impedances of the DDCC is shown in Fig. 9. It can be seen that the port Z+ of DDCC exhibits of high value parasitic resistance R_{Z+} (5.03MΩ) in parallel with low value capacitance C_{Z+} (0.024pF). Thus, the parasitic capacitance of the circuit has a small value that can be neglected in our frequency range of interest. The frequency response of the input impedance of the DDCC is shown in Fig. 10. It can be seen that the port X of DDCC exhibits of low value parasitic resistance R_X (150.2Ω) in series with low parasitic inductance L_X (4.16μH), which makes it suitable for cascading. The parasitic elements of the DDCC have been calculated in Table III. Fig. 11 shows the simulated amplitude responses of HP, LP and two BP filters with V_{i1}=V_{in} and V_{i2}=V_{i3}=0. Fig. 12 shows the simulated amplitude responses at the V_{o4} output terminal of the three-input single-output biquad. The proposed circuit was designed for f_o=1MHz and Q=1 by choosing R_1=R_2=10kΩ and C_1=C_2=15.9pF. It is observed from Figs. 11 and 12 that the simulation results agree quite well with the theoretical analysis, but the difference between the theoretical and simulated responses mainly stems from the parasitic impedance effects and non-ideal gains of the DDCC.

TABLE I. The Aspect Ratios of the CMOS Transistors in DDCC Implementation.

Transistors	L(μm)	W(μm)
M1—M4	0.36	3.6
M7—M8	0.36	5.4
M13—M20	0.18	2.52
M5—M6, M9—M12	0.18	10.08

TABLE II. Voltage and Current Transfers With f_{-3dB} Frequencies.

Transfer	DC gain	f_{-3dB}MHz
V_X/V_{Y1}	1.0000	588.84
V_X/V_{Y2}	0.9999	605.86
V_X/V_{Y3}	1.0000	574.32
I_{Z+}/I_X	0.9999	598.4

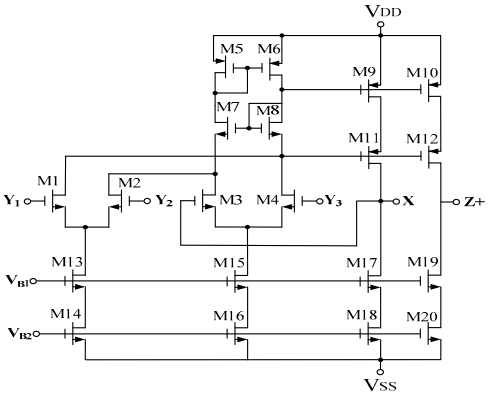

Fig. 6. The CMOS implementation of the DDCC.

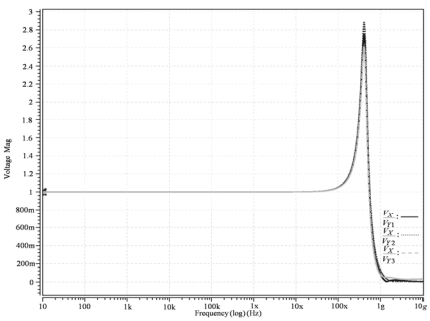

Fig. 7. Frequency response of X terminal with respect to different Y terminals.

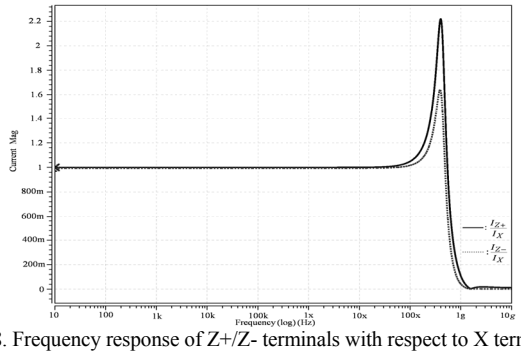

Fig. 8. Frequency response of Z+/Z- terminals with respect to X terminal.

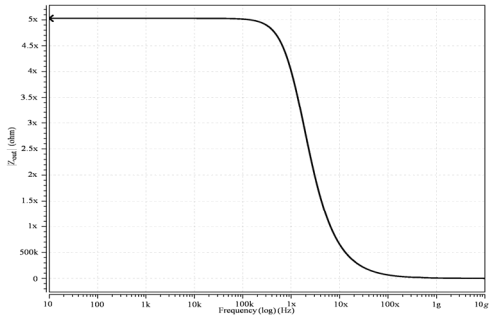

Fig. 9. Magnitude of the parasitic output impedance at Z+ terminal.

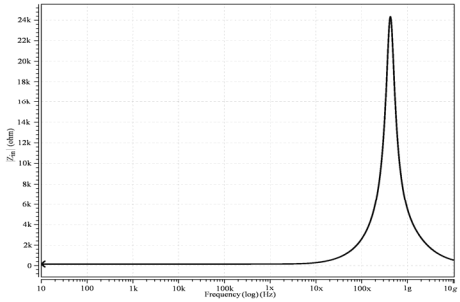

Fig. 10. Magnitude of the parasitic input impedance at X terminal.

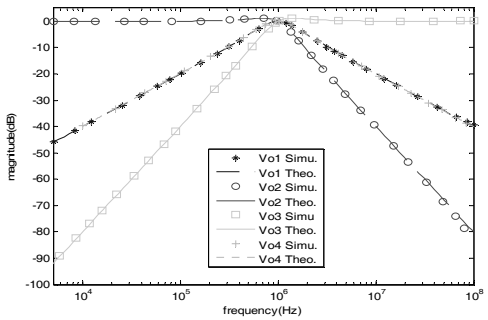

Fig. 11. The LP, HP and two BP responses of the proposed VM single input and four outputs filter.

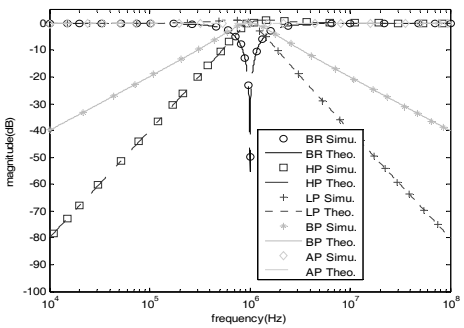

Fig 12. The LP, BP, HP, BR and AP responses of the proposed VM three inputs and single output filter.

TABLE III. PARASITIC COMPONENT VALUES OF THE DVCC.

Parasitic	Value
R_X	150.2Ω
L_X	4.16μH
C_{Y1}	3.86fF
C_{Y2}	3.86fF
C_{Y3}	0.252fF
R_{Z+}	5.03MΩ
C_{Z+}	0.024pF

VI. CONCLUSIONS

In this paper, we presented a new universal voltage-mode biquadratic filter with three inputs and four outputs. The circuit can be acted as both a multifunction voltage-mode filter with single input and four outputs and a universal voltage-mode filter with three inputs and a single output. Therefore, the circuit proposed in this paper is more versatile than the multifunction one with a single input and three outputs or the universal one with three inputs and a single output. Since the implementation configuration of the plus-type DDCC is simpler than that of minus-type DDCC, the proposed circuit employs only the plus-type DDCCs. Besides, the proposed circuit still offers the following advantages: (i) using two grounded capacitors attractive for integration and absorbing shunt parasitic capacitance, (ii) using two resistors at all X terminals of DDCCs suitable for the variations of filter parameters and absorbing series parasitic resistances at all X terminals of DDCCs, (iii) simultaneous realization of lowpass, highpass and two bandpass responses for the single-input four-output filter with high-input impedance good for cascadeability, (iv) no need to impose component choice to realize all five generic responses for the three-input single-output filter, (v) no need to employ inverting-type input signals, and (vi) low active and passive sensitivity performances. HSPICE simulation results using TSMC 0.18 μm 1P6M CMOS process technology and ±0.9V supply voltages validate the theoretical predictions.

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