DDCC-Based Tunable Voltage-Mode Multifunction Biquadrates Filter

Hua-Pin Chen, San-Fu Wang, and Yu-Ling Chang

Abstract—In this paper, a new tunable voltage-mode multifunction biquadratic filter employing two differential difference current conveyors (DDCCs) and all grounded passive elements is presented. The proposed biquadratic filter can realize highpass, bandpass and lowpass filter responses, simultaneously. The circuit offers the following advantages: (i) using grounded capacitors attractive for integration and absorbing shunt parasitic capacitances, (ii) using grounded resistors at X terminals of DDCCs suitable for the variations of filter parameters and absorbing series parasitic resistances at X terminal of DDCCs, (iii) high input impedance good for cascadability, (iv) no need to change the filter topology, (v) no need to component-matching conditions, (vi) orthogonal tunable of the resonance angular frequency and quality factor, and (vii) low active and passive sensitivity performances. HSPICE simulation results using TSMC 0.18μm 1P6M CMOS process technology and ±0.9V supply voltages validate the theoretical predictions.

***Index Terms*—Active filters, voltage-mode, analog electronics, DDCC.**

I. INTRODUCTION

At present there is a growing interest in designing analogue current-mode signal-processing circuits. In these circuits the current rather than the voltage is used as the active variable either throughout the whole circuit or only in certain critical areas [1]. The use of current-mode active devices has many other advantages such as larger dynamic, higher bandwidth, greater linearity, simple circuitry and low power consumption compared to that of voltage-mode counterparts for example operational amplifiers [1]. Filters are widely used in many communications, signal processing, automatic control, and instrumentation systems. For examples, two system block diagrams of the receiver/transmitter part of a global system for mobiles (GSM) cellular telephone and crossover network used in a three-way high-fidelity loudspeaker are introduced in [2], [3].

As a current-mode active device, the differential difference current conveyor (DDCC) has the advantages of both the second generation current conveyor (such as large signal bandwidth, great linearity, wide dynamic range) and the differential difference amplifier (such as high input impedance and arithmetic operation capability) [4]. Since the addition and subtraction operations of voltage-mode signals need the realization, respectively. The DDCC becomes very attractive to be used in the design of voltage-mode filters. This is due to the fact that the addition and subtraction operations for voltage signals can be performed easily by DDCC [4]-[11] Voltage-mode active filters with high-input impedance are of great interest because several cells of this kind can be directly connected for implementing higher order filters [7]-[15]. In 2003, Chang and Chen proposed a universal voltage-mode filter with three inputs and a single output [6]. The circuit can realize all five different generic filtering responses but only highpass (HP) and bandpass (BP) responses have the advantage of high input impedance. In 2004, Horng *et al*. proposed a multifunction filter with a single input and three outputs [7]. The circuit can realize HP, BP and lowpass (LP) responses, simultaneously. However, it suffers from orthogonal tunable of the resonance angular frequency ω_o and quality factor Q. In 2005, Ibrahim et al. proposed two single DDCC biquads with high input impedance and minimum number of passive elements [8]. The HP, BP or LP filter responses cannot be realized in the same configuration. In 2007, Chiu and Horng proposed a universal voltage-mode filter with three inputs and a single output [9]. The circuit has high-input and low-output impedances advantages but it uses three plus-type DDCCs. In the same year, Chen proposed a universal voltage-mode filter based on two plus-type DDCCs [10]. The proposed configuration suffers from high-input impedance. In 2010, Chen proposed another multifunction voltage-mode filter with single input and four outputs [11]. The circuit can realize inverting HP, inverting BP, non-inverting LP and non-inverting BP filtering functions, simultaneously. However, it suffers from orthogonal tunable of the resonance angular frequency ω_o and quality factor Q. The biquadratic filters simultaneously realizing the LP, BP and HP filtering functions have received considerable attention and finds its applications in phase locked loop FM stereo demodulators, and crossover networks used in three-way high fidelity loudspeakers [3]. Fig. 1 shows the filter application in a three-way high-fidelity loudspeaker crossover network [3].

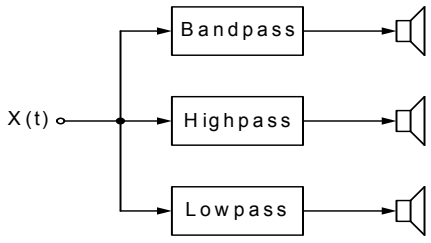


Fig. 1. The three-way high-fidelity loudspeaker crossover network [3]

In this paper, a new voltage-mode multifunction biquadratic circuit with single input and five outputs is presented. The proposed configuration employs two DDCCs, two grounded capacitors and three grounded resistors. The biquadratic filter needs neither an inverting-type voltage

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input signal nor any critical component-matching conditions to realize LP, BP and HP responses, simultaneously. The input of the circuit exhibits high input impedance so that the synthesized filter can be cascaded without additional buffers. It permits orthogonal tunability of the resonance angular frequency ω_o and quality factor Q, and enjoys low active and passive sensitivity performances. Moreover, it should be mentioned that all of the grounded resistors in the proposed filter can be replaced by electronic resistors [16] to obtain electronic tunability.

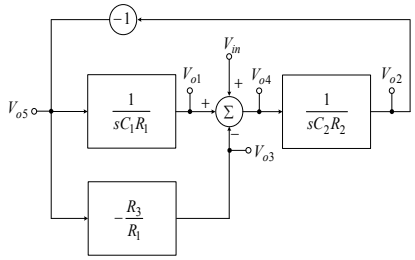


Fig. 2. Block diagram of the proposed filtering circuit.

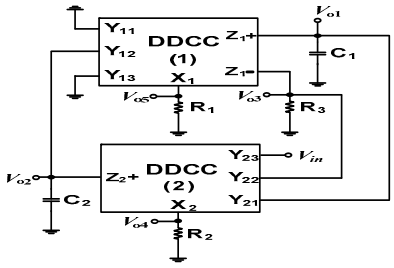


Fig. 3. The proposed tunable voltage-mode multifunction biquadratic filter.

II. Circuit Description

The block diagram representing the implementation of the single input and five outputs filtering circuit is shown in Fig. 2. The configuration consists of two lossless integrators, a proportional gain block, a summer and a voltage inverter. The summer circuit of the biquadratic filter can be implemented easily with a signal DDCC. This is due to the fact that the addition and subtraction operations for voltage signals can be performed easily by DDCC. From the diagram in Fig. 2, the implementation of the high-input impedance tunable voltage-mode DDCC-based multifunction biqaudratic circuit is shown in Fig. 3. It employs two DDCCs, two grounded capacitors and three grounded resistors. The use of grounded capacitors is attractive from monolithic integration point of view because grounded capacitor circuits can compensate for the stray capacitances at their nodes [17]. The dual-output DDCC is a six-terminal analog building block and its terminal relations are given by $I_{Y1}=I_{Y2}=I_{Y3}=0$, $V_X=V_{Y1}-V_{Y2}+V_{Y3}$ and $I_Z=\pm I_X$ [5]. Derived by each nodal equation of the proposed, the input-output relationship matrix form of Fig. 3 can be expressed as

$$\begin{bmatrix} sC_1 & G_1 & 0 & 0 & 0 \\ -G_2 & sC_2 & G_2 & 0 & 0 \\ 0 & -G_1 & G_3 & 0 & 0 \\ -1 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{o1} \\ V_{o2} \\ V_{o3} \\ V_{o4} \\ V_{o5} \end{bmatrix} = \begin{bmatrix} 0 \\ G_2V_{in} \\ 0 \\ V_{in} \\ 0 \end{bmatrix} \quad (1)$$

where $G_1=\frac{1}{R_1}$, $G_2=\frac{1}{R_2}$ and $G_3=\frac{1}{R_3}$

To derive (1), all the Y_1, Y_2 and Y_3 terminals of dual-output DDCC are high impedance terminals, since they are connected to gates of MOS devices in actual implementation, whereas the port X is low impedance terminal [5]. Similarly the two ports Z+ or Z- also exhibit high impedance since they are connected to the output stage of current mirror. From (1), the following five output voltages can be derived as

$$\frac{V_{o1}}{V_{in}}=\frac{-1}{s^2C_1C_2R_1R_2+sC_1R_3+1} \quad (2)$$

$$\frac{V_{o2}}{V_{in}}=\frac{sC_1R_1}{s^2C_1C_2R_1R_2+sC_1R_3+1} \quad (3)$$

$$\frac{V_{o3}}{V_{in}}=\frac{sC_1R_3}{s^2C_1C_2R_1R_2+sC_1R_3+1} \quad (4)$$

$$\frac{V_{o4}}{V_{in}}=\frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2+sC_1R_3+1} \quad (5)$$

$$\frac{V_{o5}}{V_{in}}=\frac{-sC_1R_1}{s^2C_1C_2R_1R_2+sC_1R_3+1} \quad (6)$$

Thus, we can obtain an inverting LP, two non-inverting BP, a non-inverting HP and an inverting BP filter responses at the output voltages, V_{o1}, V_{o2}, V_{o3}, V_{o4} and V_{o5}, respectively. Because the input voltage signal is connected directly to the Y_3 port of the dual-output DDCC(2) and input current to the Y_3 port is zero, the circuit has the feature of high input impedance. The resonance angular frequency ω_o and quality factor Q, are given by

$$\omega_o=\frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (7)$$

$$Q=\frac{1}{R_3}\sqrt{\frac{R_1R_2C_2}{C_1}} \quad (8)$$

From (7) and (8), it can be seen that the parameter Q of the proposed filter can be varied without changing the pole frequency, but not vice versa. Thus the ω_o and Q can be properly orthogonal tunability by R_1 and/or R_2 and R_3, in that order. Also, the passive ω_o and Q sensitivities are equal to or smaller than unity.

III. Effect of Non-Idealities

Taking the non-idealities from frequency dependence of internal voltage and current transfers of the dual-output DDCC into account, the relationship of the terminal voltages and currents can be rewritten as $V_X=\beta_a(s)V_{Y1}-\beta_b(s)V_{Y2}+\beta_c(s)V_{Y3}$, $I_{Z+}=\alpha_a(s)I_X$ and $I_{Z-}=-\alpha_b(s)I_X$, where $\alpha_m(s)$ $(m=a,b)$ and $\beta_n(s)$ $(n=a, b, c)$ represent the frequency transfers of the internal current and voltage followers of the dual-output DDCC. They can be approximated by the first order of low-pass functions [18].

$$\alpha_m(s)=\frac{\alpha_m}{1+\frac{s}{2\pi f_{\alpha_m}}}, \text{ for } m=a,b \quad (9)$$

$$\beta_n(s)=\frac{\beta_n}{1+\dfrac{s}{2\pi f_{\beta_n}}},\ for\ n=a,\ b,\ c \tag{10}$$

In which $\alpha_a=0.9999$, $f_{\alpha_a}=598.4\text{MH}_\text{Z}$, $\alpha_b=0.9994$, $f_{\alpha_b}=529.2\text{MH}_\text{Z}$, $\beta_a=1.000$, $f_{\beta_a}=588.84\text{MH}_\text{Z}$, $\beta_b=0.9999$, $f_{\beta_b}=605.86\text{MH}_\text{Z}$, $\beta_c=1.000$, $f_{\beta_c}=574.32\text{MH}_\text{Z}$ and using TSMC 018*u*m 1P6M CMOS process technology HSpice simulation with the parameters of lever 49 is performed. Equations (9) and (10), the pole frequencies f_{α_m} (m=*a, b*) and f_{β_n} (n=*a, b, c*) depend on the technological parameters and ideally approach infinity. The operation frequency of the presented filter can be defined as $f<<\min\{f_{\alpha_m},\ f_{\beta_n}\}$. In addition, the dc gain α_m and β_n are ideally equal to unity and can be expressed as $\alpha_m(s)=\alpha_m=1-\varepsilon_{mi}$ and $\beta_n(s)=\beta_n=1-\varepsilon_{nv}$, where ε_{mi} ($|\varepsilon_{mi}|<<1$) and ε_{nv} ($|\varepsilon_{nv}|<<1$) are the current tracking errors and the voltage tracking errors of the dual-output DDCC, respectively. Taking into account the non-idealities, Equations (2) to (6) can be rewritten as follows.

$$\frac{V_{o1}}{V_{in}}=\frac{-\alpha_{a1}\alpha_{a2}\beta_{b1}\beta_{c2}}{s^2C_1C_2R_1R_2+\alpha_{b1}\alpha_{a2}\beta_{b1}\beta_{b2}sC_1R_3+\alpha_{a1}\alpha_{a2}\beta_{b1}\beta_{a2}} \tag{11}$$

$$\frac{V_{o2}}{V_{in}}=\frac{\alpha_{a2}\beta_{c2}sC_1R_1}{s^2C_1C_2R_1R_2+\alpha_{b1}\alpha_{a2}\beta_{b1}\beta_{b2}sC_1R_3+\alpha_{a1}\alpha_{a2}\beta_{b1}\beta_{a2}} \tag{12}$$

$$\frac{V_{o3}}{V_{in}}=\frac{\alpha_{b1}\alpha_{a2}\beta_{b1}\beta_{c2}sC_1R_3}{s^2C_1C_2R_1R_2+\alpha_{b1}\alpha_{a2}\beta_{b1}\beta_{b2}sC_1R_3+\alpha_{a1}\alpha_{a2}\beta_{b1}\beta_{a2}} \tag{13}$$

$$\frac{V_{o4}}{V_{in}}=\frac{s^2C_1C_2R_1R_2+\alpha_{b1}\alpha_{a2}\beta_{b1}(\beta_{b2}-\beta_{c2})sC_1R_3+\alpha_{a1}\alpha_{a2}\beta_{b1}(\beta_{a2}-\beta_{c2})}{s^2C_1C_2R_1R_2+\alpha_{b1}\alpha_{a2}\beta_{b1}\beta_{b2}sC_1R_3+\alpha_{a1}\alpha_{a2}\beta_{b1}\beta_{a2}}$$

$$\approx\frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2+\alpha_{b1}\alpha_{a2}\beta_{b1}\beta_{b2}sC_1R_3+\alpha_{a1}\alpha_{a2}\beta_{b1}\beta_{a2}} \tag{14}$$

$$\frac{V_{o5}}{V_{in}}=\frac{-\alpha_{a2}\beta_{b1}\beta_{c2}sC_1R_1}{s^2C_1C_2R_1R_2+\alpha_{b1}\alpha_{a2}\beta_{b1}\beta_{b2}sC_1R_3+\alpha_{a1}\alpha_{a2}\beta_{b1}\beta_{a2}} \tag{15}$$

The denominator polynomial of the transfer functions of the proposed filter can be rewritten as

$$D(s)=s^2C_1C_2R_1R_2+\alpha_{b1}\alpha_{a2}\beta_{b1}\beta_{b2}sC_1R_3+\alpha_{a1}\alpha_{a2}\beta_{b1}\beta_{a2} \tag{16}$$

The non-ideal resonance angular frequency ω_o and quality factor Q are obtained by

$$\omega_0=\sqrt{\frac{\alpha_{a1}\alpha_{a2}\beta_{b1}\beta_{a2}}{R_1R_2C_1C_2}} \tag{17}$$

$$Q=\frac{1}{\alpha_{b1}\beta_{b2}R_3}\sqrt{\frac{\alpha_{a1}\beta_{a2}R_1R_2C_2}{\alpha_{a2}\beta_{b1}C_1}} \tag{18}$$

A sensitivity study forms an important index of the performance of any active network. The formal definition of sensitivity is

$$S_x^F=\frac{x}{F}\frac{\partial F}{\partial x} \tag{19}$$

where F represents one of ω_o, Q and x represents any of the passive elements or the active parameters. Based on the sensitivity expression, the active and passive sensitivities of the proposed circuit shown in Fig. 3 are given as

$$S^{\omega_o}_{\alpha_{a1},\alpha_{a2},\beta_{b1},\beta_{a2}}=-S^{\omega_o}_{R_1,R_2,C_1,C_2}=\frac{1}{2} \tag{20}$$

$$S^{Q}_{\alpha_{a1},\beta_{a2}}=S^{Q}_{R_1,R_2,C_2}=-S^{Q}_{\alpha_{a2},\beta_{b1}}=-S^{Q}_{C_1}=\frac{1}{2} \tag{21}$$

$$S^{Q}_{\alpha_{b1},\beta_{b2}}=S^{Q}_{R_3}=-1 \tag{22}$$

From the above it can be realized that even under non-ideal current and voltage gains of the dual-output DDCCs the active and passive sensitivities remain less than or equal to one in magnitude.

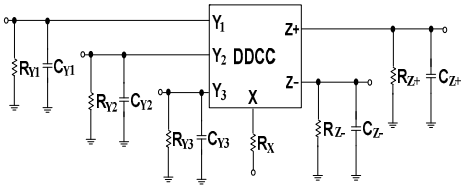


Fig. 4. Block diagram of DDCC symbol along with its parasitic elements.

IV. Parasitic Impedance Effects

The former equations from (2) to (6) have been obtained by considering ideal description of dual-output DDCCs, all the three Y terminals exhibit an infinite input resistance. The port X exhibits zero input resistance and the ports Z show an infinite output resistance. Practically when implementing the active element using transistors, these resistances assume some finite value depending upon the device parameters. Similarly, the high frequency effects also need to be accounted for by assuming capacitances at these ports. The non-ideal dual-output DDCC symbol showing various parasitic is shown in Fig. 4. It is shown that the port X exhibits of low value parasitic serial resistance R_X, the ports Y exhibit of high value parasitic resistance R_Y in parallel with low value capacitance C_Y, and the ports Z exhibit of high value parasitic resistance R_Z in parallel with low value capacitance C_Z. It is to be noted that the proposed circuit employs resistors at X terminals of the dual-output *DDCCs*, hence most of the parasitics R_X can be easily merged. To account for these non-ideal sources, the proposed circuit in Fig. 3 can be redrawn as Fig. 5 where $C_{1p}=C_{Z1+}//C_{Y21}$, $C_{2p}=C_{Z2+}//C_{Y12}$, $C_{3p}=C_{Z1-}//C_{Y22}$, $R_{1p}=R_{Z1-}//R_{Y21}$, $R_{2p}=R_{Z2+}//R_{Y12}$, and $R_{3p}=R_{Z1-}//R_{Y22}$. Note that in Fig. 5 all the grounded capacitors are connected at Z terminals of dual-output DDCCs to absorb shunt parasitic capacitances at Z terminals of dual-output DDCCs. Also, we used two grounded resistors at all X terminals of dual-output DDCCs to absorb series parasitic resistances at X terminals of dual-output DDCCs. Reanalysis of the proposed circuit in Fig. 5 the transfer functions become

$$\frac{V_{o1}}{V_{in}}=\frac{mn_1n_2}{ms^2+H_1n_2s+mn_1n_2} \tag{23}$$

$$\frac{V_{o2}}{V_{in}}=\frac{mn_2s}{ms^2+H_1n_2s+mn_1n_2} \tag{24}$$

$$\frac{V_{o3}}{V_{in}}=\frac{H_1n_2s}{ms^2+H_1n_2s+mn_1n_2} \tag{25}$$

$$\frac{V_{o4}}{V_{in}}=\frac{R_2}{R_2+R_{X2+}}\left(\frac{ms^2}{ms^2+H_1n_2s+mn_1n_2}\right) \tag{26}$$

$$\frac{V_{o5}}{V_{in}}=\frac{R_1}{R_1+R_{X1+}}\left(\frac{-mn_2s}{ms^2+H_1n_2s+mn_1n_2}\right) \tag{27}$$

where

$$n_1 = (\frac{1}{R_1^{'}})(\frac{sR_{1p}}{1+sR_{1p}C_1^{'}}) \quad (28)$$

$$n_2 = (\frac{1}{R_2^{'}})(\frac{sR_{2p}}{1+sR_{2p}C_2^{'}}) \quad (29)$$

$$m = 1+sR_3^{'}C_{3p} \quad (30)$$

$H_1 = \frac{R_3^{'}}{R_1^{'}}$, $C_1^{'} = C_1 + C_{1p}$, $C_2^{'} = C_2 + C_{2p}$, $C_{3p} = C_{Z1-} + C_{Y22}$

$R_1^{'} = R_1 + R_{X1+}$, $R_2^{'} = R_2 + R_{X2+}$ and $R_3^{'} = R_3 // R_{3p}$

Equations (28) to (30) can be rewritten as

$$n_1 = (\frac{1}{R_1^{'}C_1^{'}})(\frac{s}{s+\omega_1}) \quad (31)$$

$$n_2 = (\frac{1}{R_2^{'}C_2^{'}})(\frac{s}{s+\omega_2}) \quad (32)$$

$$m = \frac{1}{\omega_3}(s+\omega_3) \quad (33)$$

where

$$\omega_1 = \frac{1}{R_{1p}C_1^{'}} , \ \omega_2 = \frac{1}{R_{2p}C_2^{'}} \times \ \omega_3 = \frac{1}{R_3^{'}C_{3p}} \quad (34)$$

Equations (31) to (33) illustrate that the effects of the parasitic elements are dependent on three parasitic poles yielded by the non-idealities of the dual-output DDCCs. For close to ideal operation at high frequencies, the frequency of operation should be larger than ω_1 and ω_2, and smaller than ω_3. The frequency range of the proposed configuration should be restricted to the following conditions [18].

$$10f_3 \le f \le f_H = 0.1\times\min\{f_1, \ f_2\} \quad (35)$$

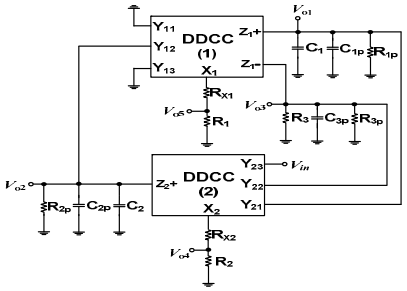


Fig. 5. The proposed tunable voltage-mode multifunction biquadratic filter including parasitics.

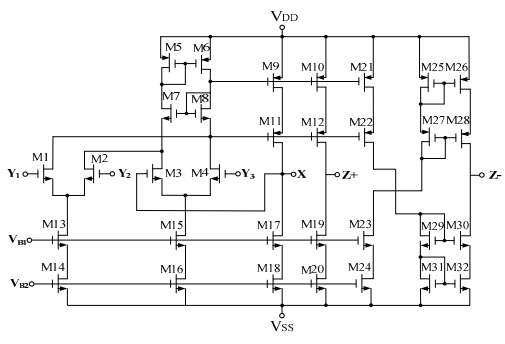


Fig. 6. The CMOS implementation of the DDCC.

TABLE I. THE ASPECT RATIOS OF THE CMOS TRANSISTORS IN DDCC IMPLEMENTATION.

Transistors	L(μm)	W(μm)
M1—M4	0.36	3.6
M7—M8	0.36	5.4
M13—M20, M23—M24	0.18	2.52
M5—M6, M9—M12, M21—M22	0.18	10.08
M25—M28	0.36	12.6
M29 —M32	0.36	7.92

V. SIMULATION RESULTS

Finally, to verify the theoretical prediction of the proposed biquadratic filter, a simulation using HSpice simulation with TSMC 0.18μm 1P6M CMOS process technology was performed and the CMOS implementation of the dual-output DDCC is shown in Fig. 6 [3]-[11]. The dimensions of MOS transistors used in implementation of the dual-output DDCC are given in Table I. The supply voltages are V_{DD}=-V_{SS}=*0.9V*, and the biasing voltages are V_{B1} and V_{B2} *-0.1 V* and *-0.36V*. The voltage follower and current follower frequency responses of dual-output DDCC are, respectively, shown in Fig. 7 and 8 which are obtained more than 100MH$_Z$. The f_{-3dB} frequencies for the voltage and current transfers are summarized in Table II. The frequency response of the output impedances of the DDCC is shown in Fig. 9. It can be seen that the port *Z*+ of DDCC exhibits of high value parasitic resistance R_{Z+} (5.03MΩ) in parallel with low value capacitance C_{Z+} (0.024pF). Thus, the parasitic capacitance of the circuit has a small value that can be neglected in our frequency range of interest. The frequency response of the input impedance of the DDCC is shown in Fig. 10. It can be seen that the port X of DDCC exhibits of low value parasitic resistance R_X (150.2Ω) in series with low parasitic inductance L_X (4.16μH), which makes it suitable for cascading. The parasitic elements of the DDCC have been calculated in Table III. By keeping the values of $R_1 = R_2 = 30\text{k}\Omega$, $C_1 = C_2 = 5.3\text{pF}$, and varying only R_3 , the quality factor Q can be controlled by following setting: $R_3 = 30\text{k}\Omega$ for *Q*=1, $R_3 = 20\text{k}\Omega$ for *Q*=1.5, $R_3 = 10\text{k}\Omega$ for *Q*=3, $R_3 = 5\text{k}\Omega$ for *Q*=6 and $R_3 = 3\text{k}\Omega$ for *Q*=10. Thus we obtain BP filter responses with different values of *Q* as shown in Fig. 11. It is important to note that high values of the *Q* can be easily obtained by varying only R_3 . By keeping the values of $C_1 = C_2 = 7.95\text{pF}$, *Q*=1, and varying only resistors $R_1 = R_2 = R_3 = R$, the pole frequency also can be tuned by following setting: $R = 10k\Omega$ for $f_0 = 2\text{MH}_Z$, $R = 15k\Omega$ for $f_0 = 1.34\text{MH}_Z$, $R = 20k\Omega$ for $f_0 = 1\text{MH}_Z$ and $R = 25k\Omega$ for $f_0 = 804K\text{H}_Z$. Thus we obtain BP filter responses with different values of f_o as shown in Fig. 12. As shown in Fig. 12, the pole frequency f_o can be adjusted without affecting the quality factor *Q*. Fig. 13 shows the simulated amplitude-frequency responses for the LP, HP and two BP filtering at V_{o1}, V_{o2}, V_{o3} and V_{o4} output terminals, with $R_1 = R_2 = R_3 = 10\text{k}\Omega$ and $C_1 = C_2 = 15.9\,\text{pF}$, leading to a center frequency of $f_o = 1\text{MH}_Z$ and quality factor of *Q*=1. It is observed from Figs. 11 to 13 that the simulation results agree quite well with the theoretical analysis, but the difference between the theoretical and simulated responses

mainly stems from the parasitic impedance effects and non-ideal gains of the DDCC.

To test the input dynamic range of the filter, the simulation has been repeated for a sinusoidal input signal at $f_o = 1\text{MH}_Z$. Fig. 14 shows that the input dynamic range of the inverting BP response at V_{o5} output terminal with $R_1 = R_2 = R_3 = 30k\Omega$ and $C_1 = C_2 = 5.3\text{pF}$, which extends up to amplitude of 0.4V (peak to peak) without signification distortion. The dependence of the output harmonic distortion of inverting BP filter on input voltage amplitude is illustrated in Fig. 15. From Fig. 15, we can see that the harmonic distortion rapidly increases if the input signal is increased beyond 0.2V for the chosen dual-output DDCC implementation.

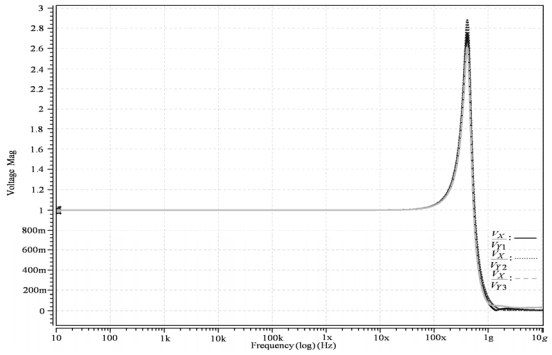


Fig. 7. Frequency response of X terminal with respect to different Y terminals.

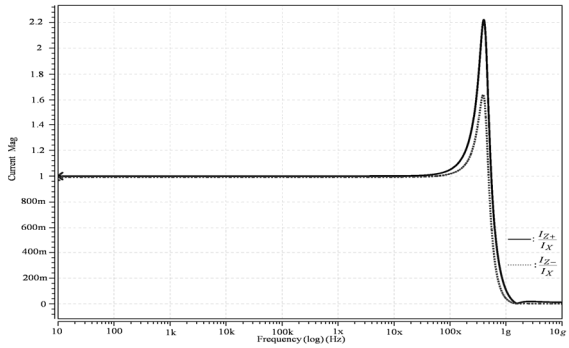


Fig. 8. Frequency response of Z+/Z- terminals with respect to X terminal.

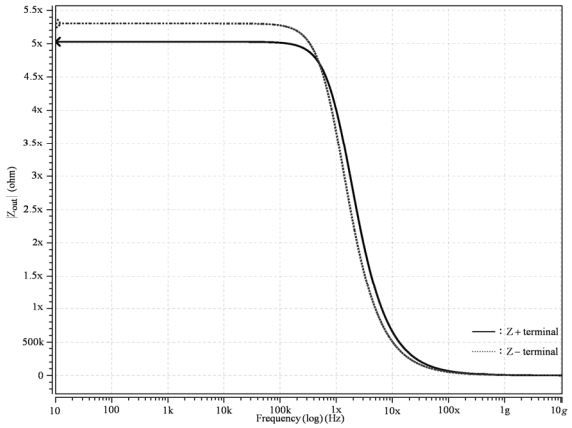


Fig. 9. Magnitude of the parasitic output impedances at Z+ and Z- terminals.

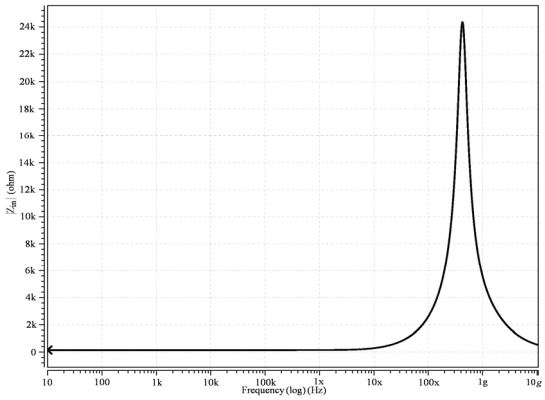


Fig. 10. Magnitude of the parasitic input impedance at X terminal.

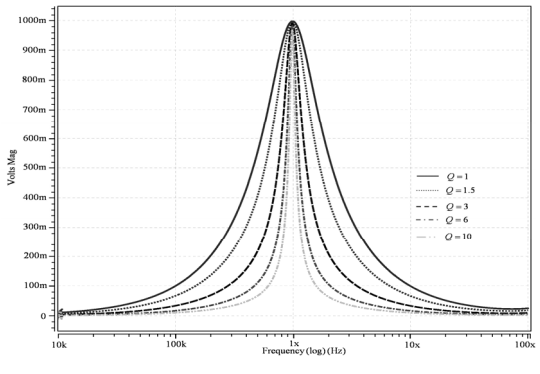


Fig. 11. Simulation results for control of Q while keeping f_o (1MH$_Z$) fixed for bandpass filter at V_{o3} output terminal.

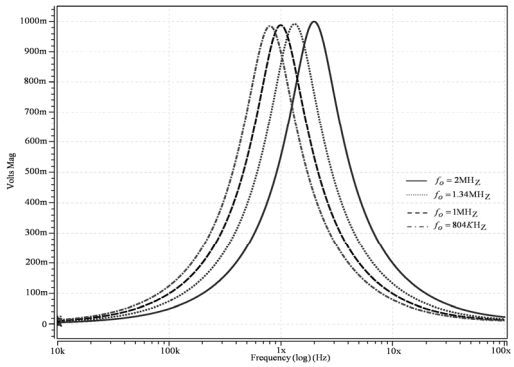


Fig. 12. Simulation results for control of fo while keeping Q (=1) fixed for bandpass filter at V_{o3} output terminal.

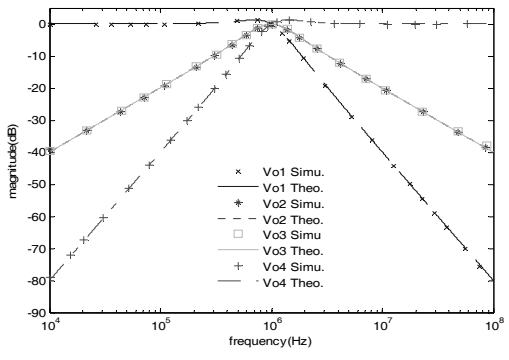


Fig. 13. Amplitude responses of the HP, LP and two BP filter.

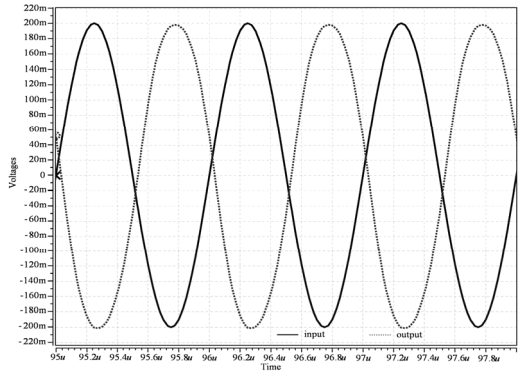


Fig. 14. The input and output waveforms of the inverting BP response at V_{o5} output terminal for a 1MHz sinusoidal input voltage of 0.4V (peak to peak).

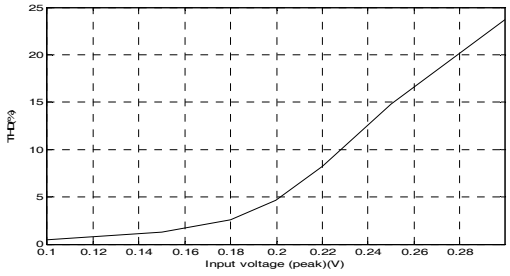


Fig. 15. Dependence of the output harmonic distortion of inverting BP filter on input voltage amplitude.

TABLE II. VOLTAGE AND CURRENT TRANSFERS WITH F-3DB FREQUENCIES.

Transfer	DC gain	f_{-3dB}MHz
V_X/V_{Y1}	1.0000	588.84
V_X/V_{Y2}	0.9999	605.86
V_X/V_{Y3}	1.0000	574.32
I_{Z+}/I_X	0.9999	598.4
I_Z/I_X	0.9994	529.2

TABLE III. PARASITIC COMPONENT VALUES OF THE DVCC.

Parasitic	Value
R_X	150.2Ω
L_X	4.16μH
C_{Y1}	3.86fF
C_{Y2}	3.86fF
C_{Y3}	0.252fF
R_{Z+}	5.03MΩ
C_{Z+}	0.024pF
R_{Z-}	5.3MΩ
C_{Z-}	0.031pF

VI. CONCLUSIONS

In this paper, the authors also propose a new high input impedance voltage-mode multifunction biquadratic filter. This circuit offers several advantages, such as simultaneous realization of LP, BP and HP filtering responses in the same configuration, no requirements for component matching conditions, the use of only grounded passive components, high input impedance, and low active and passive sensitivity performances. The proposed circuit has the same advantages reported by [11] which using two DDCCs, two grounded capacitors and two grounded resistors. Additionally, the proposed circuit has one more important advantage of orthogonal control of resonance angular frequency ω_o and quality factor Q with reported by [11]. HSPICE simulation results using TSMC 0.18μm 1P6M CMOS process technology and ±0.9V supply voltages validate the theoretical predictions.

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