A Hybrid Sequential Switching Shunt Regulator (HS3R) for Satellites

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***Abstract*—This document presents a sequential switching shunt regulator (S3R) operating with a digital shunt regulator, as hybrid configuration (HS3R) for solar array regulators. This approach describes the principles of this topology as part of a power subsystem of a lunar exploration satellite. The proposed technique is especially useful to reduce the high solar array parasitic capacitance that shows the actual satellites. The response of the HS3R is studied against large transient load changes using a hybrid configuration to reduce the losses. The results show the dynamic response of the system during each test.**

***Index Terms*—About Hybrid regulator, regulated spacecraft power system, satellite regulation system.**

I. Introduction

The sequential switching shunt regulator, S3R, has been widely used in the electrical power subsystem of satellites. The S3R provides a robust way to dissipate the exceeding solar energy during the begin-of-life of the solar panel and the periods following the eclipses, when the array is extremely cold. Since 70s the European Space Agency (ESA) has been employing the S3R for their designs [1].

The shunt regulator technology provides the required features to handle a full-regulated bus regarding the transient load changes. The S3R bring a ladder control using a hysteretic configuration to handle the shunt devices, therefore, the performance of the system can be inside of the output voltage levels required for the bus.

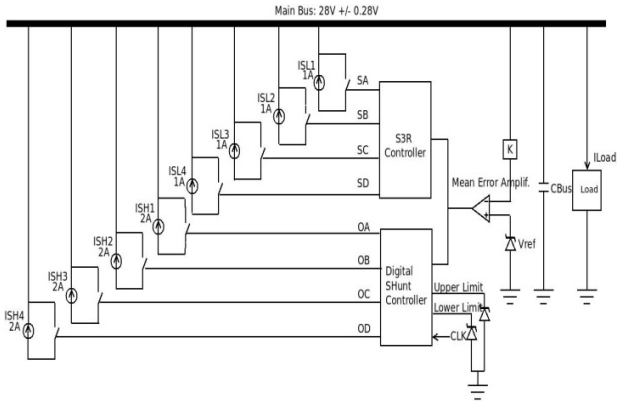


Fig. 1. Magnetization as a function of applied field.

Actually the new satellite requirements, where the new payloads uses more power, some factors, as the solar array capacitance, are generating more electrical problems. The change of technology from silicon to GaAs triple junction also shows high parasitic capacitance, around five times larger than its predecessor over the same voltage and power ratings [2]-[5].

The impact of this parasitic capacitance represents some drawbacks that must be resolved [6]; some of them are summarized as follows:

- Increase switching power losses in the shunt transistor.
- Larger turn-on delay in the shunt transistor.

Accordingly to the problems just stated, the aim of this work is to present a S3R topology that overcomes it. The idea uses the S3R technique with a digital shut regulator, to create a hybrid power regulator, or HS3R.

II. Control Strategy

The implementation of a hybrid sequential switching shunt regulator, HS3R, mainly focus On an integrated operation between the S3R controller and the digital shunt regulator. To performance this technique, the solar arrays must be divided in two section, a lower power section, ISL1~4, and a high power section, ISL1~4, as in Fig. 1.

Using the error signal coming from the mean error amplifier, MEA, the system can measure the output load changes, and decide what control mode is adequate for that instant. The possible modes during the operation are: minimum load perturbation, small load perturbation and high load perturbation.

The S3R controller handles the lower power solar array sections, using a sequential switching arrangement of hysteric comparators. Every comparator has an established voltage reference, once that voltage is overpassed by the MEA signal the following comparator is activated, as ladder configuration.

The digital shunt controller compares the MEA signal against to voltage references, a upper limit and a lower limit. These two reference acts as triggers of the high power solar array sections. The S3R voltage reference has been located inside of these two limits in order to have a group operation that permits to handle greater demands, changing the operation of S3R to hybrid mode. Fig. 2 represents the graphical behavior of this topology.

The control strategy employed in this work is described as follows:

- During the time t_0-t_1, the system is under a minimum load perturbation that only generates a modulation inside of the S3R limits. In this mode the system is switching (between A1~A2 limits) only with the first low power solar array section, ISL1, while the last three sections are disconnected from the bus.
- From t_1-t_2 the system is working under a small load perturbation, using the S3R controller, it can be noted

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its operation during small changes of the load current. The first and second low power sections are connected to the bus, and the third section is now switching, while the last section is not operating. This method is a sequential switching process, which provides more current to the load when is needed. The digital shunt controller still not working.

- After t_2, a large load perturbation requires more current that the S3R controller can provide. In this moment the MEA signal overpasses the upper limit to activate the first high-power solar array section, this condition permits to decrease the voltage rating of the MEA signal, making possible to come back to the S3R mode. The system still have the chance to handle more load requirement due to the system has three more high-power solar sections deactivated. A master clock is required to guarantee the how many sections must be turned-on or turned-off.

The system operation is related with the instant load requirement, where the commutation devices are activated following a sequential configuration to guarantee that only one transistor is working at the time. This sequential operation is easily observable in the Fig. 2, where the mean error signal. MEA, is increasing along with the load requirements.

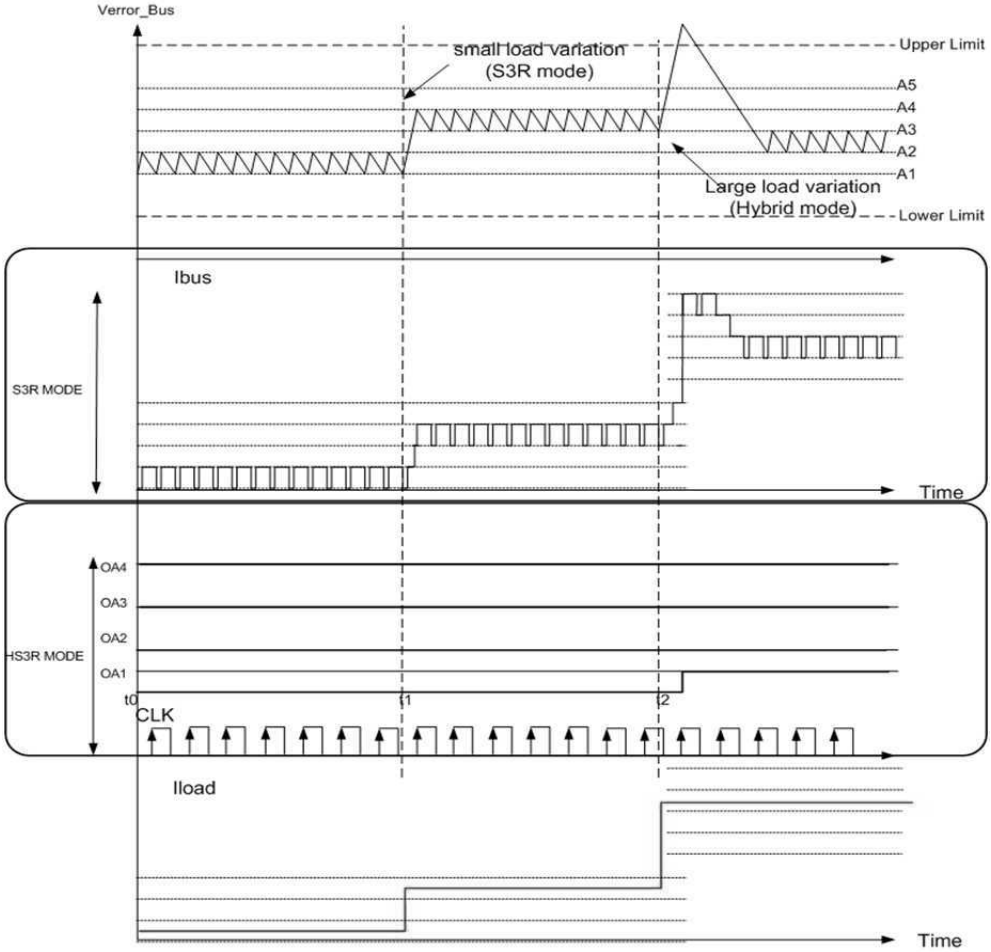


Fig. 2. Control Strategy. a) Mean error amplifier (MEA) signal, b) S3R mode, c) HS3R mode, d) Clock signal and e) Load current.

Under the HS3R mode, it can be appreciated the ON/OFF function of the transistors regarding the principle of only one transistor is switching at the time. In this way the high power section operated under this mode, reduces the problematic switching power losses.

The MEA and HS3R modes in this work uses four solar array sections each one. This condition permits to make modular systems with upgradeable capabilities to supply higher load requirements.

III. Simulation Results

The system specification are summarize in the Table I:

The system has been tested against different load variations to check its behavior. The implementation of this work was made using Pspice 16.2. The configuration uses 8 current sources, as solar array section substitutes, four of 1A and four of 2A. The load variations are programmed in the simulation software to test every mode described in the control strategy section. The load variation goes from 0.75A to 6.5A, depending on the test.

The results are presented regarding every operation mode that the system can tolerate.

A. Minimum Load Perturbation

During this mode the system was tested with a very low load perturbation in the range of 1.10A~1.40A. The bus remain inside of its nominal value, and only is appreciated a change of the modulation frequency during the load current increment. The fig. 3, presents the graphic of the main bus voltage, the load current, the mean error amplifier control signal, where this signal remain using one solar array section. The last four signal correspond to the digital shunt controller

that is turned-off.

This period is special useful to demonstrate the operation of this topology against very low changes and its behavior in this steady state.

TABLE I: HS3R SPECIFICATIONS OF THE CONFIGURATION

HS3R Specifications	
Parameter	**Value**
Bus voltage	28 V
Power cells (SAS)	4 x Low Power Section 4 x High Power Section
Low Power Solar Array Section	1A
High Power Solar Array Section	2A
Bus voltage ripple (ΔVBUS)	< 1% VBUS
Output impedance (Zo max)	< 250 mΩ
Bus capacitance	500 μF

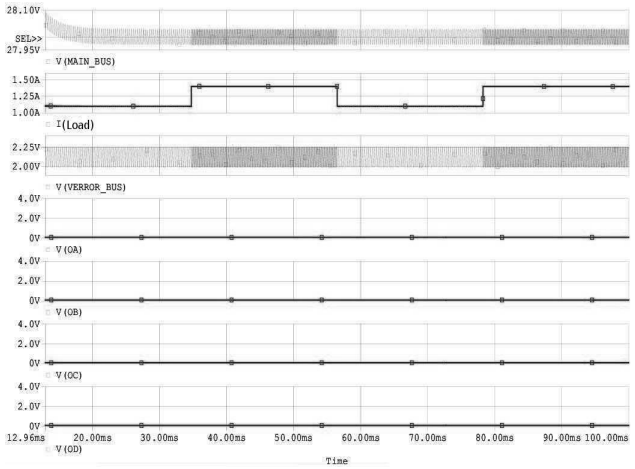


Fig. 3. Minimum load perturbation. a) Main bus voltage, b) Load current, c) MEA signal, d) Digital shunt controller signals.

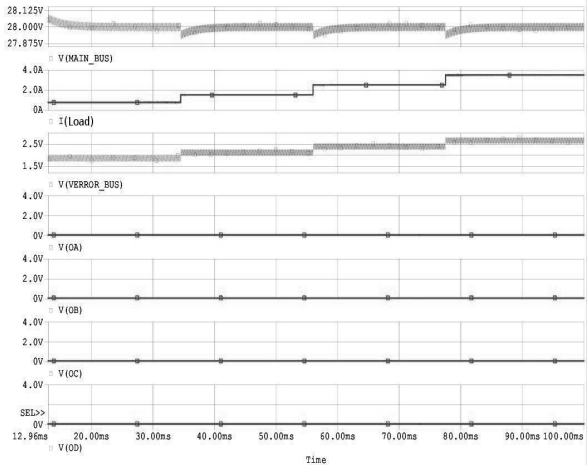


Fig. 4. Small load perturbation. a) Main bus voltage, b) Load current, c) MEA signal, d) Digital shunt controller signals.

B. Small Load Perturbation

During this mode the system is operated under small load current variations. The variable load was programmed to make an incremental variation from 0.75A to 3.5 A. The fig. 4, displays this results. The mean error amplifier signal shows the ladder behavior of the S3R controller, when a current variation appears this controller begins to use the following solar array section. This configuration permits to only one transistor to be operating in a switching mode, meanwhile the others remain turned on and/or off. The digital shunt controller still not working, due to the small load requirements are not reached the activation or high limit.

C. Large Load Perturbation

During this mode the system works under large current changes. The implementation of this test uses a load variation with a large incremental current configuration, from 0.75A to 6.5A in six steps and one final decremental step of 2.9 A. These results are displayed in the Fig. 5.

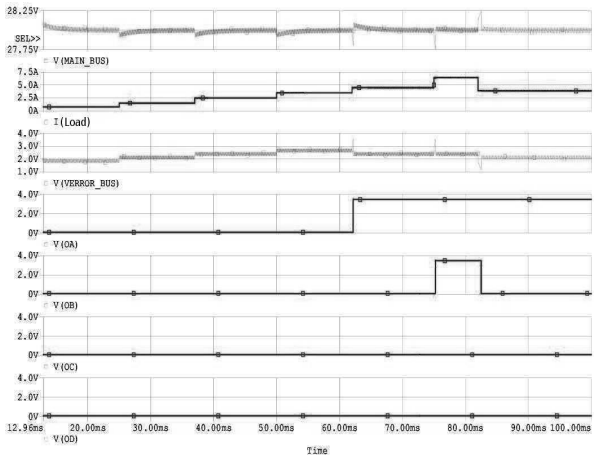


Fig. 5. Large load perturbation. a) Main bus voltage, b) Load current, c) MEA signal, d) Digital shunt controller signals.

During the first four steps the system operates using the S3R controller. In the fifth step the requirement overpasses the S3R capabilities, in that moment the digital shunt controller begins to operate turning-on a high power section, called hybrid operation. The sixth step requires more current, as the previous step, the system reacts and the second high power sections is also tuned-on. In the final step, a decrement in the current load is appreciated, the system using the mean error amplifier signal determines that is not needed anymore to have turned-on the second high power section.

The large perturbation can be seen in the MEA signal where high transients overpass the S3R limits, generating a hybrid operation.

In a similar way, the system performs the vice-versa operation, where the load requirements decrease to a minimum value. To performance the power reduction, the system must wait for the mean error amplifier signal goes under the "low limit" and turn-off one of the high-power solar array sections.

IV. CONCLUSIONS

The HS3R provides a way to handle more power reducing the switching power losses and the turn-on delay in the shunt transistors. The results demonstrated the operation of the hybrid regulator regarding the bus voltage nominal value at every current load changes. All the advantages of the basic technology, the S3R, are maintained under this topology, as the sequential operation that enables only one transistor

switching at the time.

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